Technology development and analysis of a multiphysic system based on NEMS co-integrated with CMOS for mass detection application

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THÈSE

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To my family, my colleagues and my friends for their supports
Thank you! Merci beaucoup!

"It's a MEMS MEMS MEMS world"[1]

[1]Inspired from the song *"It's a man's man's man's world"* from James Brown, recorded in New York in 1966.

Contents

Abstract

During these last decades, Very Large Scale Integration (VLSI) techniques, well developed for transistors, have been used for the Micro ElectroMechanical Systems (MEMS) devices. Thanks to the combination of different physical properties (such as electronic, mechanical, optical etc.) the fabrication of various kinds of miniaturized sensors has been made possible. The sub-µm downscaling of MEMS has allowed the emergence of a new kind of devices called NEMS (for Nano ElectroMechanical Systems) and the possible use of the electromechanical systems in specific applications in which a high level of sensitivity and resolution is necessary, such as gas sensing, mass spectrometry and molecules recognition, to replace traditional bulky machines. Nevertheless, the use of these NEMS requires a CMOS electronic to enhance NEMS resonators readout and to implement closed-loop oscillators (e.g. phase-locked loop or self-oscillating loop) that provide real-time mass measurements. The integration of the electronic circuit with the resonators is a critical aspect for the fabrication of high performance sensors. The best way consists in monolithically processing these two parts on the same die allowing a size reduction of the sensor and an optimal signal transmission between the NEMS resonators and the CMOS circuit. In a first time, this thesis proposes to analyze the interest of this co-integration from an electrical point of view. In a second time, this thesis deals with the development of a 3D co-integration in which the nano-resonators are fabricated above the CMOS circuit and the interconnections. The final part is focused on the layout design considerations for the implementation of a compact mass sensor based on a NEMS array co-integrated with a CMOS.

Résumé

Ces dernières décennies ont vu l'émergence des microsystèmes électromécaniques (MEMS) grâce notamment aux techniques de fabrication employées dans l'élaboration des transistors. L'utilisation de différentes propriétés physiques (électroniques, mécaniques, optiques par exemple) a permis la construction d'un large panel de capteurs miniaturisés. Résultant de la miniaturisation sub-micrométrique des MEMS, les nanosystèmes électromécaniques (NEMS) constituent un tout nouveau type d'objet permettant d'adresser des applications nécessitant un très haut niveau de sensibilité et de résolution, comme la détection de gaz, la spectrométrie de masse ou la reconnaissance de molécules faisant traditionnellement appel à des machines très volumineuses. L'utilisation de ces NEMS requiert cependant un circuit électronique CMOS afin de lire et d'exploiter le signal en sortie de résonateur et servant également à la mise en place d'une boucle oscillante (boucle à verrouillage de phase ou boucle auto-oscillante par exemple), architecture idéale pour la détection de masse en temps réel.L'intégration du circuit CMOS avec les résonateurs NEMS constitue un aspect critique quant à la fabrication de capteurs de haute performance. La solution optimale consiste à intégrer de manière monolithique ces deux parties sur la même puce, permettant ainsi de réduire la dimension du capteur et d'améliorer la transmission du signal électrique entre les résonateurs et le circuit CMOS. Cette thèse propose dans un premier temps d'analyser l'intérêt de cette co-intégration du point de vue électrique. Dans un second temps, cette thèse portera sur le développement d'une approche originale visant à co-intégrer de manière monolithique les nano-résonateurs au-dessus du circuit CMOS et des interconnexions. La dernière partie portera sur le design d'un détecteur de masse composé d'un réseau compact de NEMS co-intégré CMOS.

List of Symbols

2D	Two dimensional
3D	Three dimensional
AMI	Acoustic Micro Imaging
APCVD	Atmospheric Pressure Chemical Vapor Deposition
BAW	Bulk Acoustic Wave
BE (or BEOL)	Back End Of Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BOX	Buried OXide
CAE	Computer Aided Engineering
C-C	Clamped-Clamped
C-F	Clamped-Free
C-Si	Monocrystalline silicon
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing/Planarization
CVD	Chemical Vapor Deposition
D2D	Die to die
D2W	Die to wafer
DLP	Digital Light Proccessing
DMD	Digital Mirror Device
DRIE	Deep Reactive Ion Etching
DUV	Deep Ultra Violet
ECD	Electro-Chemical Deposition
FE (or FEOL)	Front End Of Line
FIB	Focused Ion Beam
GC	Gas Chromatography
HF	Hydrofluoric acid
IC	Integrated Circuit
ISFET	Ion Sensitive Field Effect Transistor

ITRS	International Technology Roadmap for Semiconductors
KOH	Potassium Hydroxide
KOZ	Keep-Out-Zone
LIGA	**LI**thographie **G**alvanoformung **A**bformung (Lithography, electroplating and molding)
LOCOS	LOCal Oxidation of Silicon
LPCVD	Low Pressure Chemical Vapor Deposition
LSI	Large Scale Integration
MagFPWs	Magnetically-actuated flexural plate wave
ME	Middle End
MEMS	Micro Electro Mechanical Systems
NEMS	Nano Electro Mechanical Systems
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
PZR	Piezoresistive
RIE	Reactive Ion Etching
RTP	Rapid Thermal Process
SAM	Scanning Acoustic Microscopy
SAW	Surface Acoustic Wave
SEM	Scanning Electron Microscopy
SBR	Signal-to-Background Ratio
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SiP	System in Package
TEOS	Tetra Ethyl Ortho Silicate
TLP	Transient Liquid Phase
TMAH	Tetra Methyl Ammonium Hydroxide
TSV	Through Silicon Via
VLSI	Very Large Scale Integration
VOC	Volatile Organic Compound
W2W	Wafer to wafer

General Introduction

During these last decades, Very Large Scale Integration (VLSI) techniques, well developed for transistors, have been used for Micro ElectroMechanical Systems (MEMS) devices. Thanks to the combination of different physical properties (such as electronic, mechanical, optical etc.), the fabrication of various kinds of miniaturized sensors and actuators has been made possible, making these electromechanical systems present everywhere in our daily life, for example in our cars (airbag, pressure sensors) or in our smartphones (microphones, accelerometers) etc. In the 2000's, the sub-µm downscaling of MEMS has led to the emergence of a new kind of devices called NEMS (for Nano ElectroMechanical Systems). Although these nanometer size devices do not pretend to the same application as the micrometer size systems, they feature outstanding properties making possible the use of NEMS in specific applications in which a high level of sensitivity and resolution is necessary, such as gas sensing, mass spectrometry and molecules recognition, to replace traditional bulky machines.In this context, an electronic circuit, which can be manufactured using a CMOS technology,is necessary for the constitution of a real-time sensor for two main reasons:

- To enhance NEMS resonators readout;
- For the implementation of closed-loop oscillators (e.g. phase-locked loop or self-oscillating loop) that provide real-time mass measurements.

The integration of the electronic circuit with the resonators constitutes a critical aspect for the fabrication of high performance and compact sensors.

The work presented in this manuscript was performed in the frame of an ERC project (European Research Council) so-called DELPHINS (Design and ELaboration of multi-Physics Integrated NanoSystems). Its main goal consists in building a generic multi-sensor design and technology platform for embedded on-chip multi-gas analyzers, based on arrays of NEMS resonators as sensing devices. This thesis presents an original technological implementation in order to achieve this purpose.

The first chapter of this manuscript introduces the global context of M/NEMS devices, followed by an overview of different solutions for mass detection application. The working principle of mass sensing with NEMS resonators will also be explained. In a final part, the different methods to integrate NEMS with CMOS circuit will be presented.

In chapter II, the signal transmission properties of different interconnection techniques are analyzed and compared in order to select the most suitable strategy for the implementation of NEMS-based mass sensors. The main results of electrical characterizations of an experimental co-integrated NEMS-CMOS device are afterwards presented. A modeling of this system is introduced and used to extract the resonator parameters and performances. From the model and the electrical results, an experimental demonstration of a simple and compact self-oscillating loop is presented.

Chapter III will report on a novel method to implement a mass detector using a 3D co-integration in which NEMS resonators are monolithically fabricated above both the CMOS circuit and the interconnections. The process flow and the main technological modules of this development will be explained in detail.

Before the conclusion, chapter IV will briefly provide guidelines to optimize the layout of CMOS-integrated NEMS arrays.

Chapter I

Micro and Nano Electro Mechanical Systems
Key objects to implement high performance sensor

Micro and Nano ElectroMechanical Systems, also known as M/NEMS (also called micromachines in Japan or MST for Micro Systems Technology in Europe), correspond to objects at the micro and nano-scale dimension using not only the electronic but also other physical properties, such as mechanical, thermal, optical, magnetic and so on. Historically, the main material for these M/NEMS objects has been silicon since it constitutes a low-cost material (abundant element on Earth) and combines outstanding electronic and mechanical properties. Furthermore the silicon processes used for the electromechanical systems elaboration are the same as those used in microelectronics for the fabrication of CMOS (Complementary Metal Oxide Semiconductor) transistors. Consequently, electromechanical structures constitute very attractive objects because of their potential in Very Large Scale Integration (VLSI) and their compatibility with the CMOS technology.

This chapter first proposes to introduce the history of the M/NEMS objects and to present their current economic impact. After that, this manuscript will focus on the mass detection application. This part will overview existing devices for such applications and will explain how M/NEMS can be used for this purpose. Then, the chapter will describe the way to design and fabricate M/NEMS-based mass sensor. Finally, some fabrication strategies will be described and overviewed, allowing the selection of the most suitable approach for mass detector fabrication using electromechanical systems.

I. Introduction

This chapter will start with a general overview of micro and nano electromechanical systems. This part is important in order to clearly define the scientific and industrial context around this device, its evolution from the first ideas to the last advanced productions and its future in terms of commercialization and technological improvements.

I.1 Context

By analyzing the electronics research field from the second part of the 20th century until now, arrival and presence of M/NEMS objects in our daily life could be premeditated. The idea of this "Infinitesimal Machinery" [Fey93] was discussed first by Richard Feynman in one of his lectures in 1959 who will initiate the nanotechnology area [Fey92].

The last sixty years have seen the major development of the electronic field. Based on the first macroscopic prototype of the transistor produced in 1947, microelectronic devices have emerged. By paving the way of various and promising applications, this field moved to into the industrial production in the beginning of 1950's. Since 1965, the Moore's law[2] has driven microelectronics improvements, more particularly the CMOS technology. As a consequence, electronic chips contain more and more transistors which become more and more tiny year after year. This trend is however confronted with physical and economic cost limits of development. The transistor dimensions cannot be scaled down indefinitely. Although its production is possible (but expensive), its work principle differs and belongs to quantum regime making it impossible to use for current computing application. However, other strategies have been developed allowing new possibilities and new applications (presented in Figure I.1.1). The so-called *"More than Moore"* approach proposes to integrate other functionalities in the electronic chip, such as sensing devices. Made commonly with silicon or with basic materials from the CMOS technology, these mechanical structures use the same fabrication technology as electronic circuits'.

[2]Gordon Moore is an American businessman and co-founder of Intel Corporation. He is also famous for its Moore's law which predicts the number of transistors inside integrated circuits per year.

Taking advantage of the low-cost production, the VLSI possibility and the compatibility with the CMOS technology, these electromechanical systems appear as very attractive objects for the semiconductor industries, and more particularly for the sensor manufacturing[3].

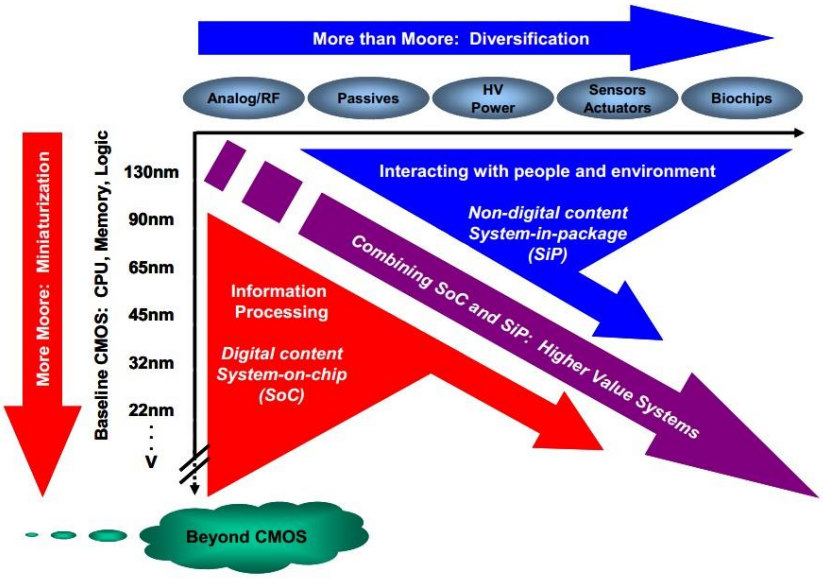


Figure I.1.1 :"More Moore vs More than Moore" representation. This schematic depicts the major trends of microelectronic and microsystems devices [ITR10].

I.2 Brief history

One on the first "miniature" electromechanical sensor was made in 1959 by the Kulite Corporation [Kul] who commercialized the first piezo-resistive silicon based pressure sensors [Tog97]. Nevertheless, the resonant gate transistor from the team of Mr. Nathanson made in 1965 is considered as the first electromechanical system using surface micromachining techniques [Nat65]. This device (presented in Figure I.1.2) was made in gold and manufactured using silicon technology. [Nat67] reports its characteristics: a 32 kHz resonator with beam length, width, thickness respectively of 480µm, 13µm, 3µm and a beam-to-substrate gap of 4µm by using a resist as sacrificial layer to release the mechanical structure. Although this device pioneered the MEMS field, the term of Micro Electromechanical System (MEMS) will only be introduced 21 years later by the Defense Advanced Research Projects Agency, so-called DARPA, an agency of the United States Department of Defense, in charge of the development of new technologies for military use [DAR-DARb].

[3] More information about technological trend in microelectronics is available in the ITRS website [ITR13].

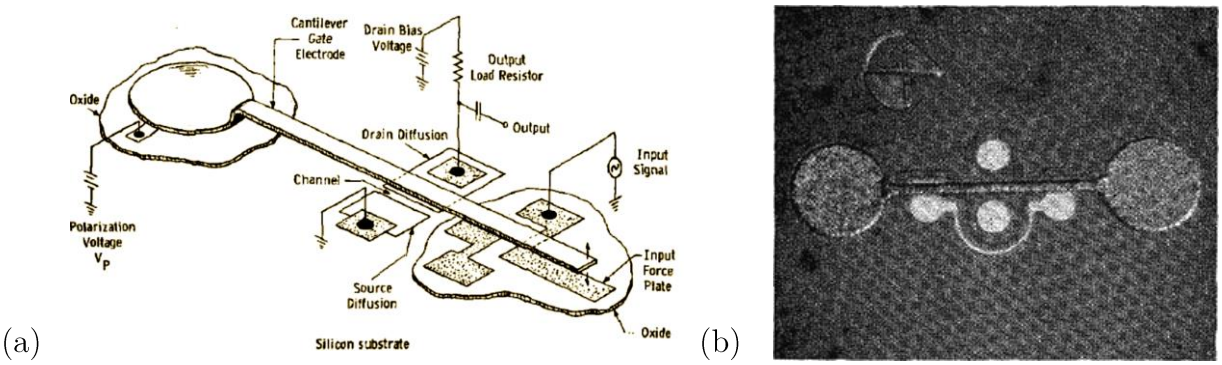


Figure I.1.2: First MEMS development: the resonant gate transistor. In (a) is presented a schematic description of a clamped-free (C-F) beam, in (b) is shown a photography of a clamped-clamped (C-C) device [Nat67].

The first studies of silicon-based structural layer combined with oxide-based sacrificial layer for surface micromachining are performed during the 1980s [How82-Pet82] which will lead to the first IC-compatible surface micromachining process [How83]. In the same period specific technological processes dedicated for microsystems development have emerged, such as specific isotropic and anisotropic silicon etching respectively in 1959 [Rob59] and in 1962 [Hol62-Tel94], direct and anodic wafer bonding respectively in 1966 [Nak66] and 1969 [Pom69], LIGA in 1982 [Bec82-Mad02-Sai09], DRIE in 1994 [Lae96]. This last one was the starting point of TSVs and three dimensional (3D) stacking technology developments.

All of these techniques have paved the way of a wide variety of devices either in academic or industrial field: pressure sensor produced by Honeywell in 1984 [Guc84], [Pet85] and K. Petersen from IBM in 1988 [Pet88], inkjet printing heads from HP [Ham84] and IBM [Pet79] in 1979, monolithic Digital Light Processing (DLP) technology from Texas Instrument in 1987 with the first Digital Micro-mirror Device (DMD) projector commercialized around 1997 [Hor96] and so on.

In parallel of these devices commercialization the 90's constitute a major period for the electromechanical system development with the creation of the first foundries and CMOS compatible MEMS processes dedicated to MEMS fabrication. MUMPs (Multi-User MEMS Process) from Cronos in 1993 and SUMMiT (Sandia Ultra-Planar, Multi-level MEMS technology) from Sandia National Laboratories in 1998 are the first examples of MEMS fabrication processes. The MCNC (Microelectronics Center of North Carolina) has extensively contributed to the development of these technologies [Mar95].

This compatibility with CMOS technology will lead during the same period to the first hybrid MEMS-CMOS systems implementations. For example, in 1992, the University of Michigan developed a MEMS-CMOS mass flow sensor [Yoo92] (Figure I.1.3). Analog Devices in collaboration with the University of California (UC) Berkeley developed and commercialized one of the first inertial sensor integrated with BiCMOS circuit which will be used in airbag systems [Rie93] (Figure I.1.4). This

integration strategy allows the development of tiny sensors with the possibility to incorporate several of them on a single chip.Sandia National Laboratories in 1995 [Smi95] developed a MEMS-CMOS pressure sensor using their M³EMS technology (Figure I.1.3). During the 1990's and 2000's, many universities and companies worked in this research field, companies such as Analog Devices, Infineon, Honeywell, IBM, Bosch, Texas-Instrument, and research and development centers such as UC Berkeley, university of Michigan, Carnegie Mellon University, Massachusetts Institute of Technology (MIT), Fraunhofer Institute, the Swiss federal institute of Technology (ETH) in Zürich.

Since 2000, several groups have studied the sub-µm downscaling of MEMS. This size reduction has allowed the emergence of new kind of objects different from micrometric devices, and the possible use of electromechanical systems in specific applications requiring a high level of sensitivity, like mass detection. The first researchers having studied NEMS (Nano-Electro Mechanical System) field are the groups of Prof. H. G. Craighead from Cornell University [Cra00] and Prof. M. L. Roukes from Caltech [Rou01], [Eki05]. The term "nano" indicates that two out of the three main dimensions are sub micrometric. In Figure I.1.5 are compared dimensions of micro and nano electromechanical systems with some biological entities for a better understanding.

Thus, all these facts allow to understand the reasons of pervasiveness of MEMS in our daily life. Indeed, the discovery and improvement of fabrication techniques, the transition from bulk micromachining to surface micromachining, the creation of MEMS foundries and processes, the compatibility with CMOS technology which have lead to CMOS-MEMS integration and MEMS miniaturization have made the use of these devices essential for numerous applications.

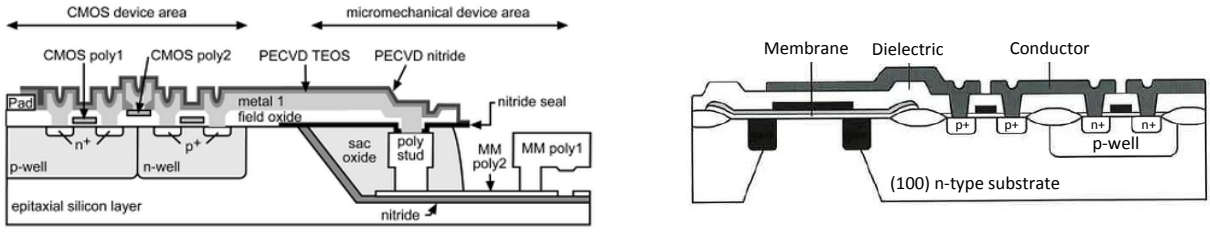


Figure I.1.3: Cross-sectional schematic of an integrated MEMS-CMOS chip from M³EMS technology developed by Sandia National Laboratories (on the left) [Smi95-Bra05], and from the University of Michigan (on the right) [Yoo92-Bra05]. These devices are one of the first examples of integrated MEMS-CMOS devices.

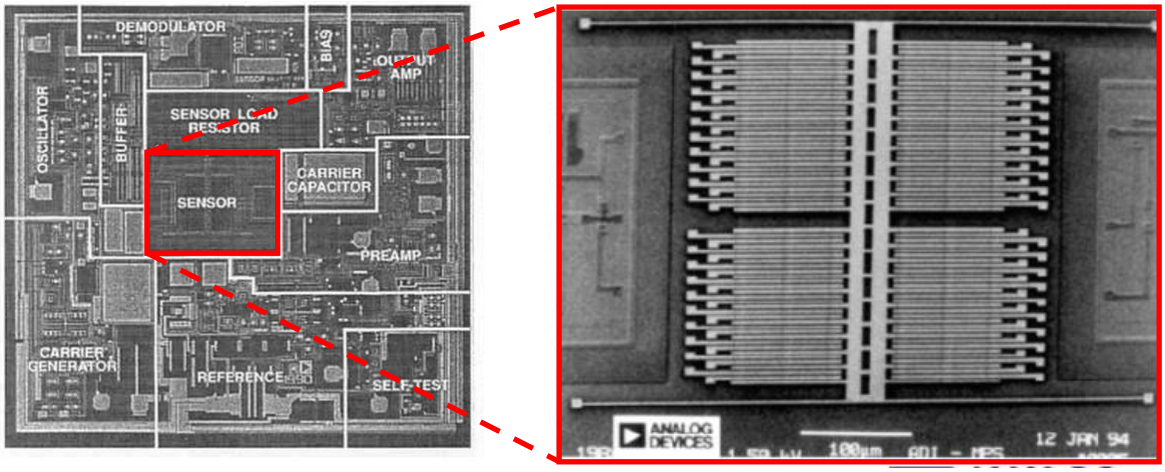


Figure I.1.4: Micrograph of the ADXL50 accelerometer (on the left) with a zoom on the sensing element (on the right). The MEMS is integrated with BiCMOS electronics on the same chip. The latter is 3mm x 3mm and is one of the first integrated MEMS-CMOS commercialized chips [Rie93]. It was particularly used in airbag technology (images modified from [NRC97]).

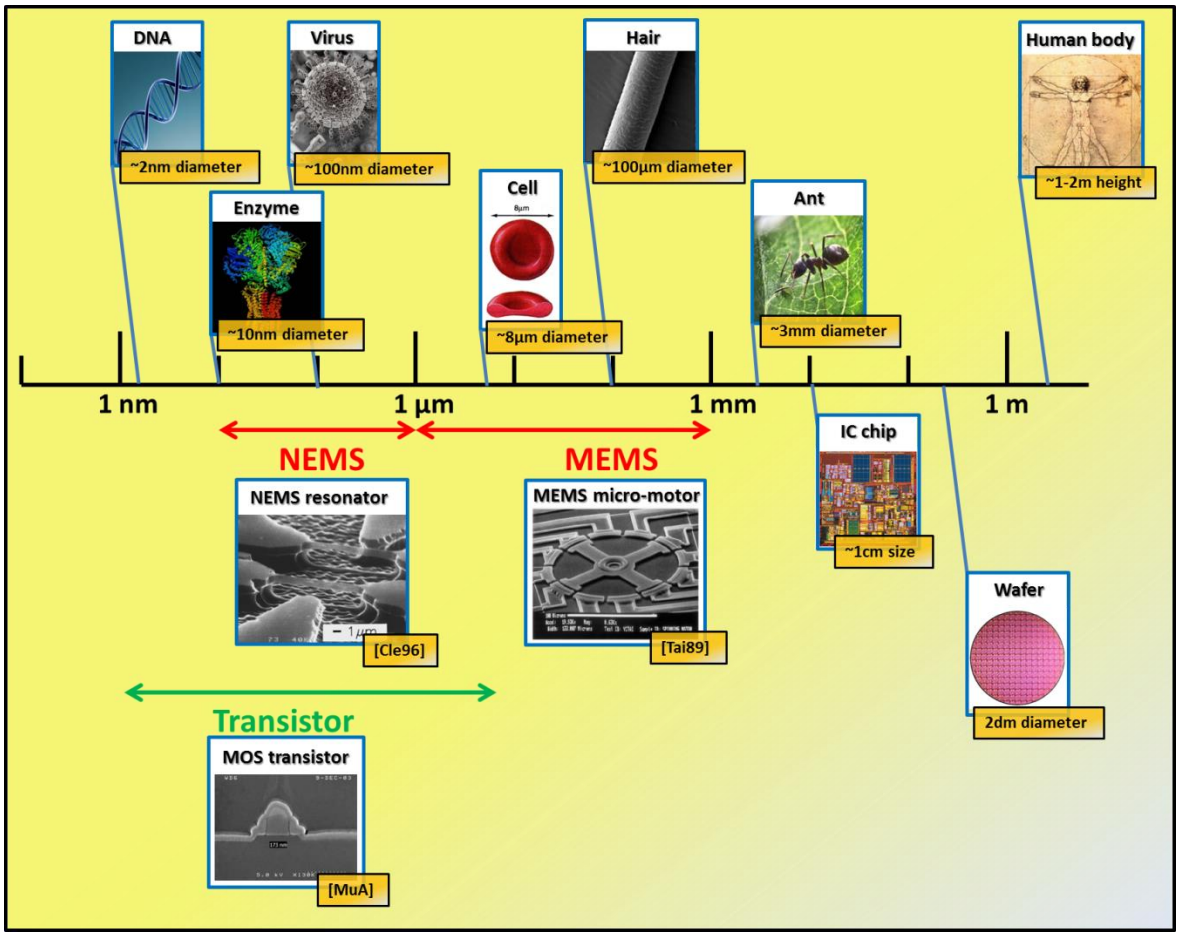


Figure I.1.5. Schematic of dimensional comparison between biological (up) and microelectronic (down) systems.

I.3 MEMS vs NEMS

The basis of the system architecture of M/NEMS-based sensors is common to many types of sensors. The central element of such a system is a single or an array of movable elements in physical interaction with its environment. This interaction can take several forms: acceleration, particles, light irradiation, magnetic and electric field exposition and so on. Its movement is then measured by an electromechanical detection stage which converts a mechanic motion into an electrical signal. The latter may be analyzed with the use of an electronic circuit (Figure I.1.6). These MEMS devices can be present through different types (*i.e.* microsensors, ASIC and microactuators) depending on the application, as described in Figures I.1.7 and I.1.8.

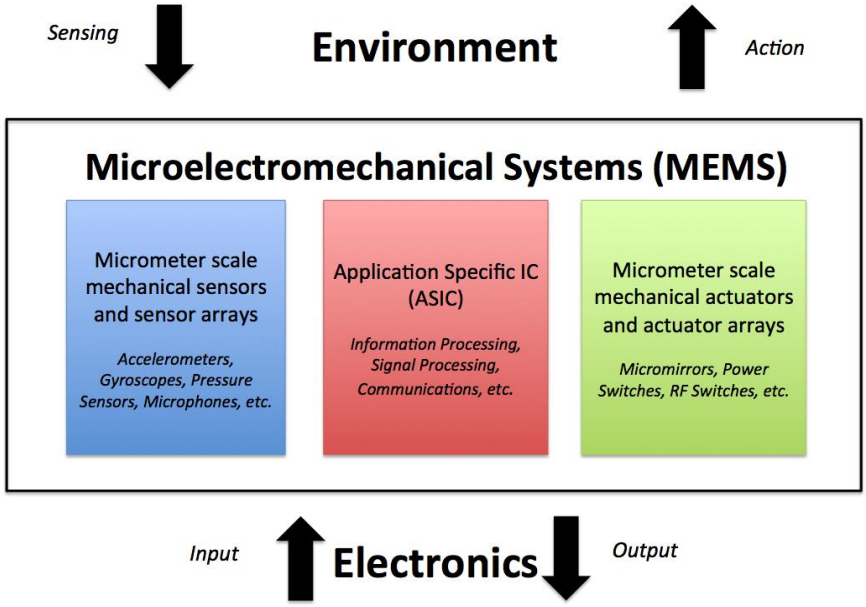


Figure I.1.6: Functionality diagram of a MEMS device [ITR13].

As a consequence of micrometric electromechanical devices miniaturization, NEMS constitute innovative objects and are strongly different from MEMS devices. Both of these systems do not pretend for the same application because of their characteristics. Indeed, MEMS are usually used as seismic mass for inertial sensors, such as accelerometers [Lem11], gyroscopes [Wal12] and magnetometers [Ett11]. These systems are sensitive to inertial forces due to their mass, unlike NEMS devices. Dimensions and low-mass of these latter make them enough sensitive to detect minute changes in their environment like small mechanical stress variation or particles detection. Robert *et al.* have reported an accelerometer sensor development using an approach called *M&NEMS*, combining MEMS as inertial mass and NEMS as suspended strain gauge at the same time [Rob09]. Typical dimension range for both MEMS and NEMS is given in Figure I.1.5.

This downscaling implies a reduction of the Volume to Surface Ratio and the predominance of surface forces (Figures I.1.9 and I.1.10). This constitutes an issue for mechanical structure integrity, particularly during the release process (see Chapter III).

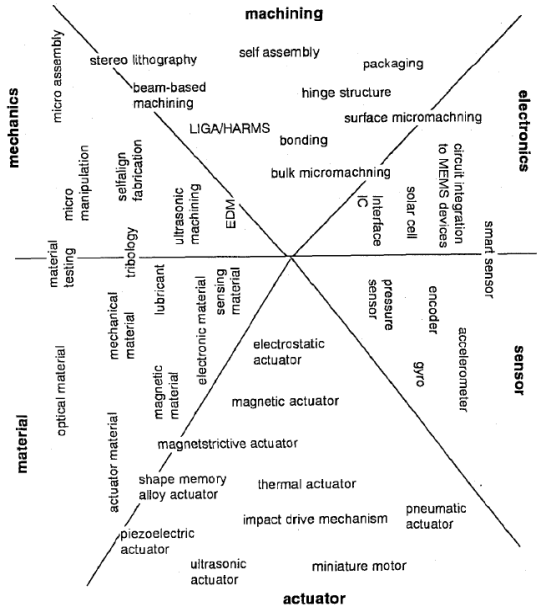


Figure I.1.7: A large panel of MEMS devices... [Fuj97]

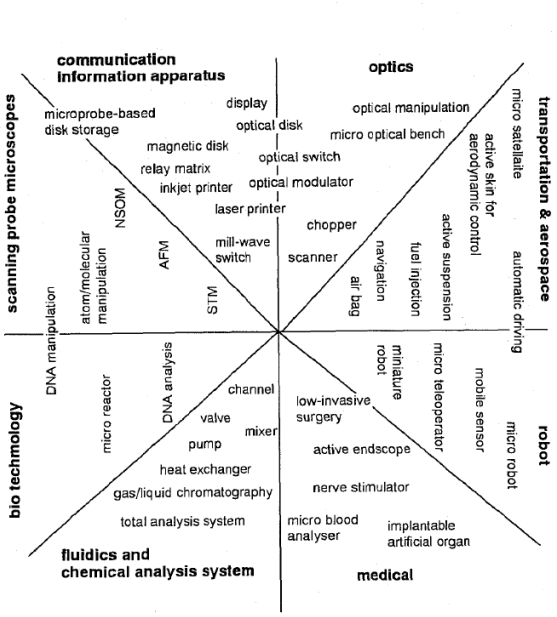


Figure I.1.8: ... for a large variety of applications [Fuj97].

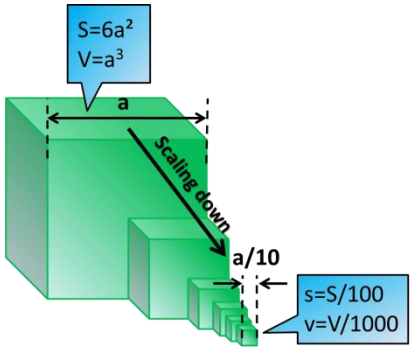


Figure I.1.9: Effect of miniaturization on surface area (S and s) and volume (V and v).

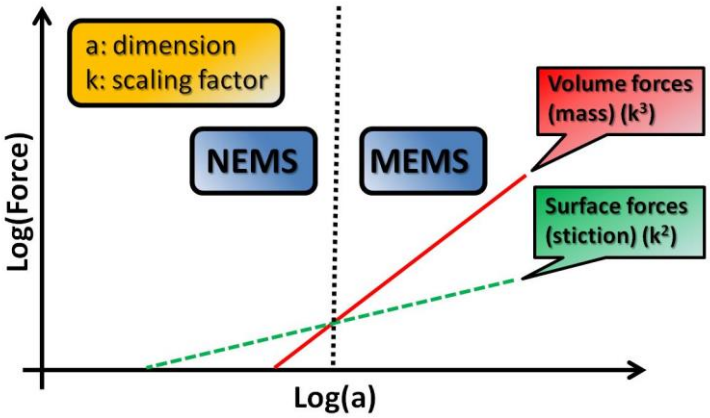
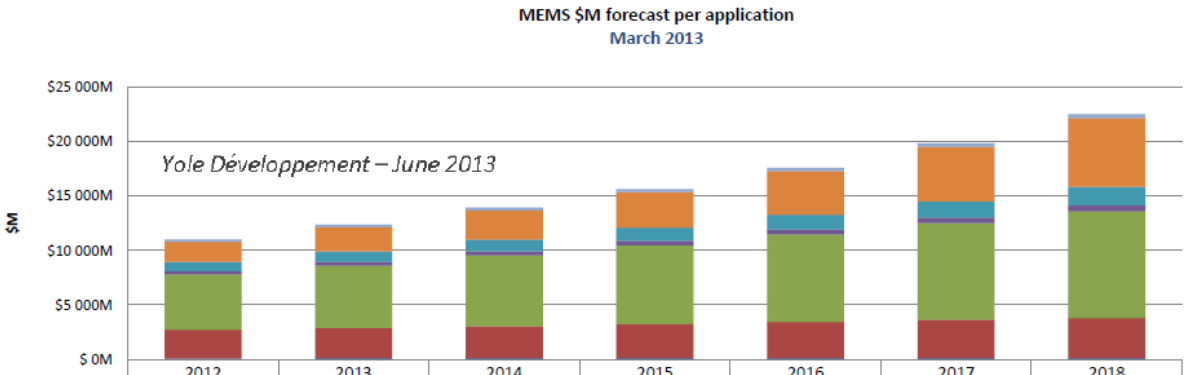


Figure I.1.10. Representation of the downscaling effect on physical phenomena. a corresponds to the main dimension of the object and k is the scaling factor.

I.4 About the market

An analysis of the place taken by MEMS in market and economic field is necessary to understand the importance of electromechanical devices. In Figure I.1.11 and Figure I.1.12 are respectively represented the MEMS market evolution over time according to different fields and the 30 most important MEMS companies in 2011. As depicted in Figure I.1.11, MEMS market is in constant increase and should continue to grow up. Automotive and consumer (such as tablets, smartphones, video games etc) constitute the two major markets of MEMS. Figures I.1.13 and I.1.14 respectively show the high use of MEMS in automotive field (control of mechanical elements, navigation, security of drivers and car passengers etc) and the economic context for some specific devices. But the most important segment is now the consumer field. The market context is depicted in Figure I.1.15. Two typical examples are depicted in Figure I.1.16. Thanks to the use of MEMS-based accelerometers, Nintendo with *Wii* and Apple with the *iPhone* have introduced the most important use of MEMS in our daily life and have drastically increased their revenues.

Electromechanical systems at the nano-scale dimensions are still under development and start to be commercialized. Further miniaturization leads to new kind of applications requiring high sensitivity and resolution level which can be explored now, like mass detection for example.



	2012	2013	2014	2015	2016	2017	2018
Telecom	$ 188M	$ 210M	$ 239M	$ 265M	$ 297M	$ 329M	$ 364M
Medical	$1 835M	$2 205M	$2 688M	$3 277M	$4 021M	$4 981M	$6 304M
Industrial	$ 874M	$ 963M	$1 069M	$1 203M	$1 339M	$1 495M	$1 676M
Defense	$ 297M	$ 335M	$ 379M	$ 421M	$ 470M	$ 525M	$ 583M
Consumer	$5 048M	$5 752M	$6 487M	$7 216M	$7 999M	$8 833M	$9 776M
Automotive	$2 639M	$2 760M	$2 934M	$3 115M	$3 322M	$3 503M	$3 643M
Aeronautics	$ 107M	$ 115M	$ 124M	$ 134M	$ 143M	$ 152M	$ 156M

Figure I.1.11: Bar chart depicting the growth of the MEMS market by market segment.
Source: Yole Development Status of MEMS Industry 2013.

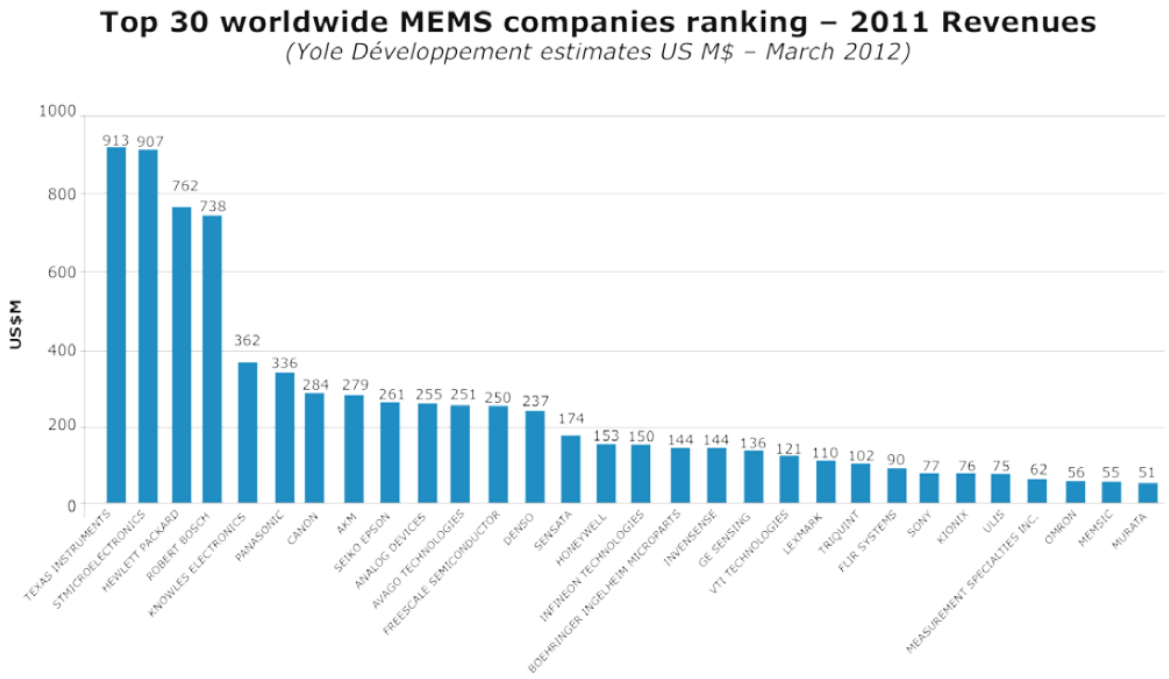


Figure I.1.12: Bar chart of the 30 top worldwide MEMS companies in terms of 2011 revenues. Source: Yole Development Status of MEMS Industry presented at MEMS Industry Group's M2M Forum May 8-10, 2012, Pittsburg PA.

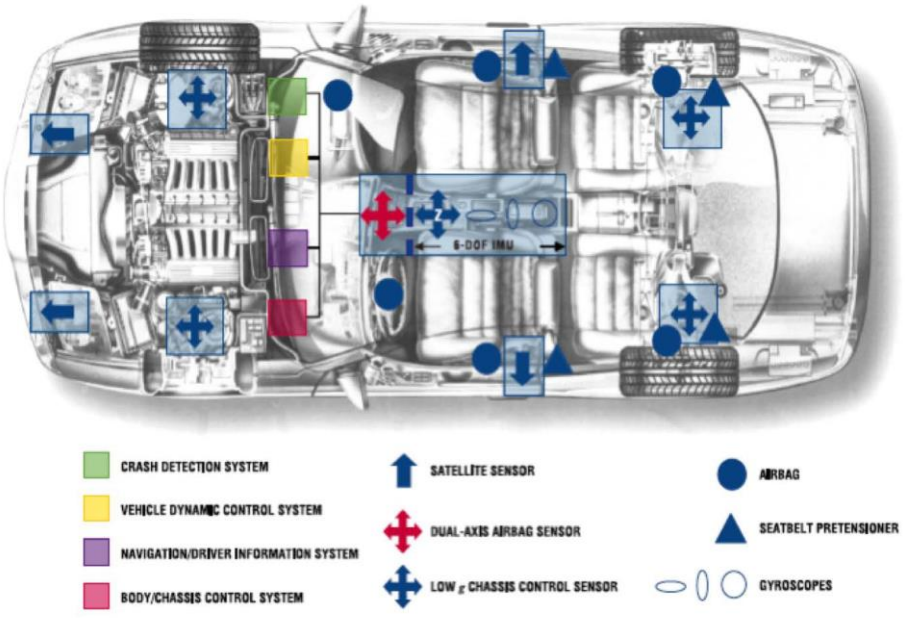
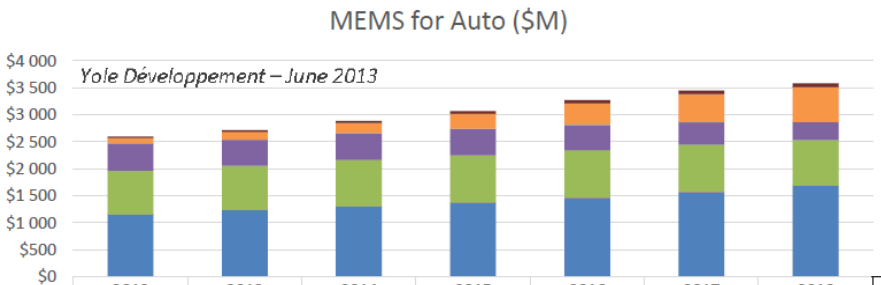


Figure I.1.13: Schematic illustration of the huge MEMS presence in automotive applications [ITR13].

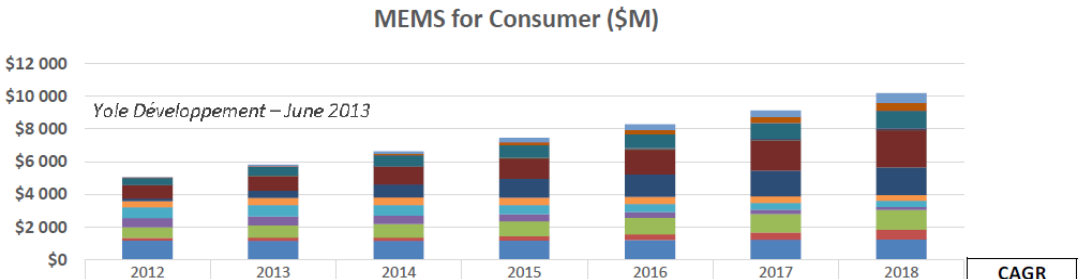
MEMS for auto will grow from $2.6B in 2012 to $3.6B in 2018 with a 5% CAGR.



	2012	2013	2014	2015	2016	2017	2018	CAGR
Micro bolometers	$21	$28	$34	$44	$59	$65	$76	23%
Optical MEMS	$0	$0	$0	$0	$0	$1	$1	44%
IMUs	$106	$147	$192	$280	$394	$516	$641	35%
Magnetometers	$5	$5	$5	$5	$5	$6	$6	2%
Gyros	$502	$480	$493	$485	$463	$413	$331	-7%
Acceleros	$806	$820	$855	$872	$882	$872	$841	1%
Microphones	$1	$1	$2	$2	$3	$4	$5	32%
Pressure	$1 159	$1 238	$1 309	$1 378	$1 464	$1 572	$1 686	6%

Figure I.1.14: Bar chart depicting the growth of the MEMS market in the automotive field for different devices (CAGR for Compound Annual Growth Rate and IMU for Inertial Measurement Unit). Source: Yole Development Status of MEMS Industry 2013.

MEMS for consumer will grow from $5B in 2012 to $9.6B in 2018 with a 11% CAGR.



	2012	2013	2014	2015	2016	2017	2018	CAGR
Others	$3	$61	$140	$270	$333	$409	$591	140%
Oscillators	$29	$44	$85	$164	$265	$374	$467	59%
RF MEMS	$439	$555	$674	$773	$863	$970	$1 087	16%
Microdisplays	$4	$4	$10	$23	$54	$78	$104	73%
PIR & Thermopiles	$12	$14	$16	$18	$20	$22	$25	13%
Optical MEMS	$814	$907	$1 088	$1 259	$1 520	$1 836	$2 259	19%
Inertial combos	$163	$451	$803	$1 159	$1 379	$1 577	$1 699	48%
Magnetometers	$357	$426	$462	$457	$439	$389	$348	0%
Gyros	$668	$698	$644	$555	$485	$426	$372	-9%
Acceleros	$574	$543	$499	$426	$348	$266	$186	-17%
Microphones	$642	$762	$836	$914	$1 008	$1 120	$1 202	11%
Pressure	$162	$190	$208	$267	$359	$459	$610	25%
IJHeads	$1 175	$1 153	$1 153	$1 173	$1 204	$1 217	$1 234	1%

* « Others » includes: energy harvesting, micro structures, humidity sensors in consumer, touchscreens, chemical MEMS / gas sensors in consumer, microfuel cells, micro speakers

Figure I.1.15: Bar chart depicting the growth of the MEMS market in their consumer field for different devices. Source: Yole Development Status of MEMS Industry 2013.

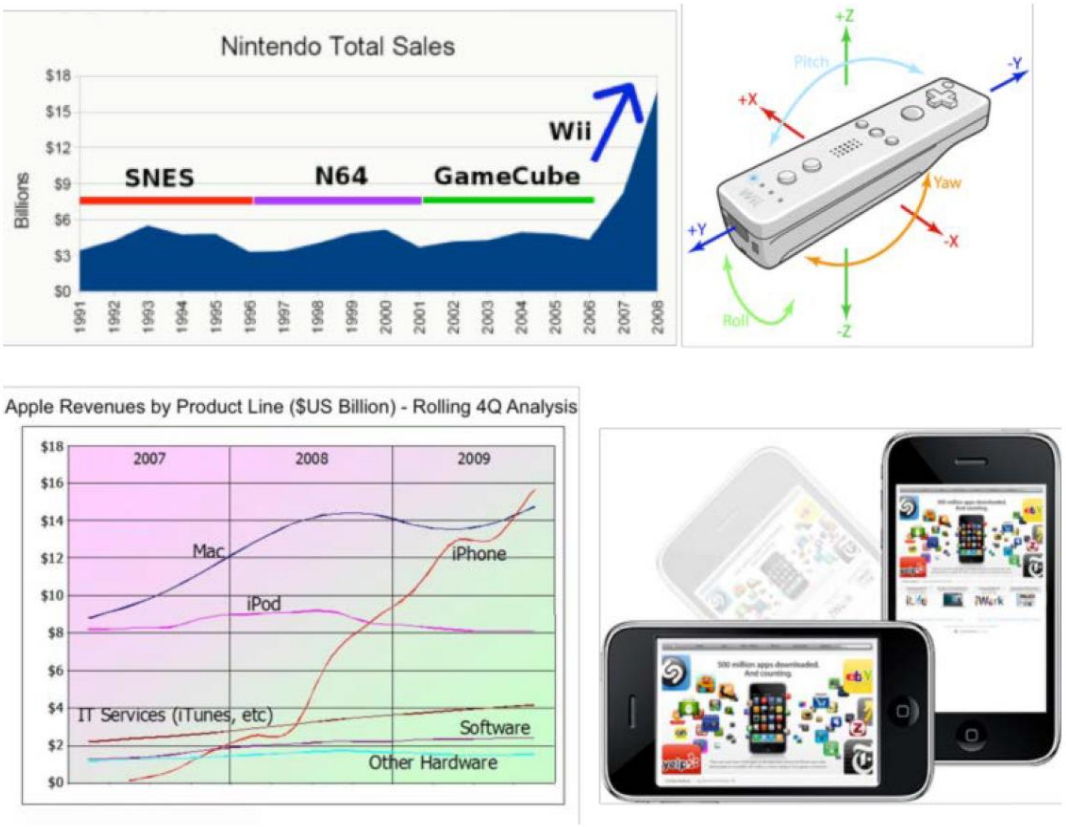


Figure I.1.16: Illustration of MEMS impact on consumer application. Nintendo's revenue (top left) has strongly increased since the commercialization of Wii using MEMS accelerometer technology in *Wii* (top right). Same phenomenon is present for Apple: its annual revenue has strongly increased from 2007 to 2009 since the introduction of *iPhone* which uses MEMS accelerometers for their display technology (bottom left and right) [ITR13].
Sources: http://www.straferight.com
http://www.osculator.net/
http://itcandor.net/2010/02/01/apple-results-q409/
http://askiphone.net/locking-your-iphone-screen-in-portrait-vertical-orientation/

II. NEMS-based mass sensor

The previous part demonstrated the important use of MEMS as sensors thanks to the combination of its physical properties. Many functions have been proposed: from pressure sensors to accelerometers etc. This part will now focus on mass detection applications, such as gas sensing and mass spectrometry. A brief overview of commercialized devices is proposed for a comparison with NEMS-based resonators. Finally the working principle of NEMS resonator implemented as gas sensor will be described.

II.1 Overview of different commercialized mass detectors

II.1.1 – Gas sensors

The main goal of these devices consists of the determination of the nature and concentration of different species inside a gas mixture. A lot of implementations can be found in the state-of-the-art using different detection techniques, e.g. field effect detection with ISFETs [Ber70] or GasFETs [Lun75], acoustic method with SAW [Woh79] and BAW [Jos02] sensors, IR-sensor [DET], micro-thermal conductivity detector (µTCD) [Kaa09-Kaa10] etc. Some of them are used to detect one particular molecule and others to detect several gas species. On same development a functionalization of the sensor is required, and in others a chromatographic stage to separate and differentiate the different species is implemented.

A "golden standard" device for chemical analysis is depicted in Figure I.2.1 coming from Agilent technologies [AGI]. It allows both a separation of the different components of a gas mixture and concentration quantification of each species. Although its sensitivity is quite impressive (<< 1 amu[4]), this system is really massive, bulky, expensive and has to be connected to a laboratory environment. Besides it shows a high consumption in terms of both power (hundreds of Watt) and time (10 to 30 minutes per analysis).

[4] amu stands for atomic mass unit and corresponds to approximately 1.6605×10^{-27} kg

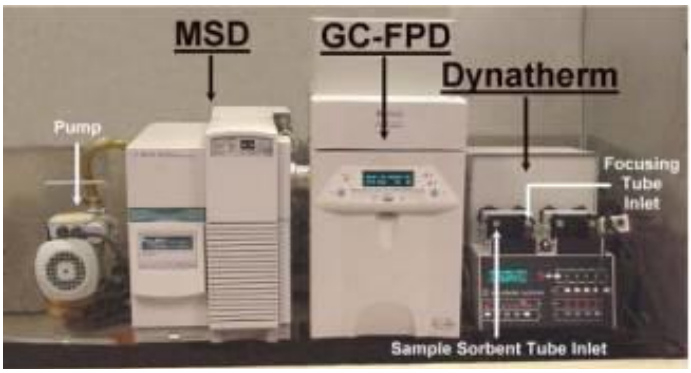
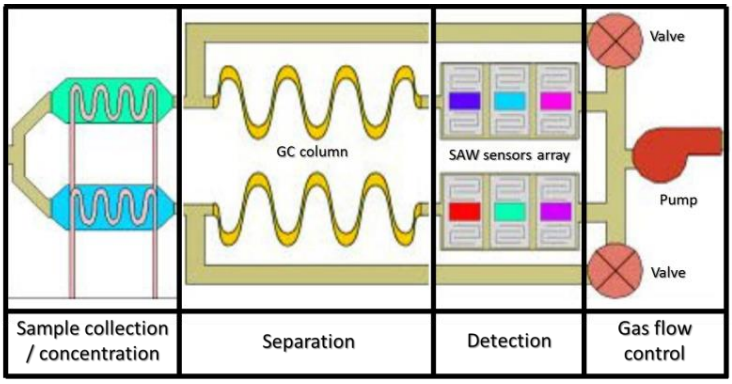


Figure I.2.1: Photography of a commercial system from Agilent technologies for gas analysis [AGI]. MSD and GC-FPD respectively stand for Mass Selective Detector and Gas Chromatography – Flame Photometric Detection

Sandia National Laboratories have implemented a more portable gas analysis system called "MicroChemLab". It monolithically integrates a sample collection and concentration stage followed by a GC column-based separation step and an array of several SAW sensors array for detection. The schematic and photos of the chip and packaged system are provided in Figure I.2.2. A large variety of gas species can be detected. This implementation constitutes a remarkable example of gas sensor: this device presents a low-cost fabrication, a 2min analysis cycle (for one analysis), a tiny size (2.8mm x 6.3mm), low power consumption (0.6W maximum), a high resolution (10ng of DMMP achieved) and sensitivity (0.11 ng/°).

(a)



(b)

(c)

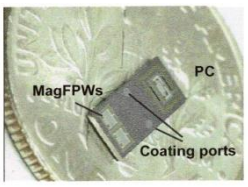


Figure I.2.2: (a) Schematic of the MicroChemLab, portable gas analysis system proposed by Sandia National Laboratories; (b) Photography of such a system with package; (c) Photography of the monolithic chip using Magnetically-actuated flexural plate wave (MagFPW) sensors [SAN]; [Lew06]. PC stands for planar preconcentrator.

Other examples of embedded gas detector devices exist (shown in Figure I.2.3). All of them rely on electronic nose (e-nose) architecture [Ars04-Pat11] because of their specificity, unlike the previous examples. Indeed they are developed for detecting only one type of molecules by using several measurement techniques, such as piezo-resistive micro-cantilevers [Pin07], electrochemical sensors [MAD], photoionization detector (PID) [CYR] with a high precision (until a concentration of 1 ppb for [CYR]) and a detection in real-time (20s for [SMI]).

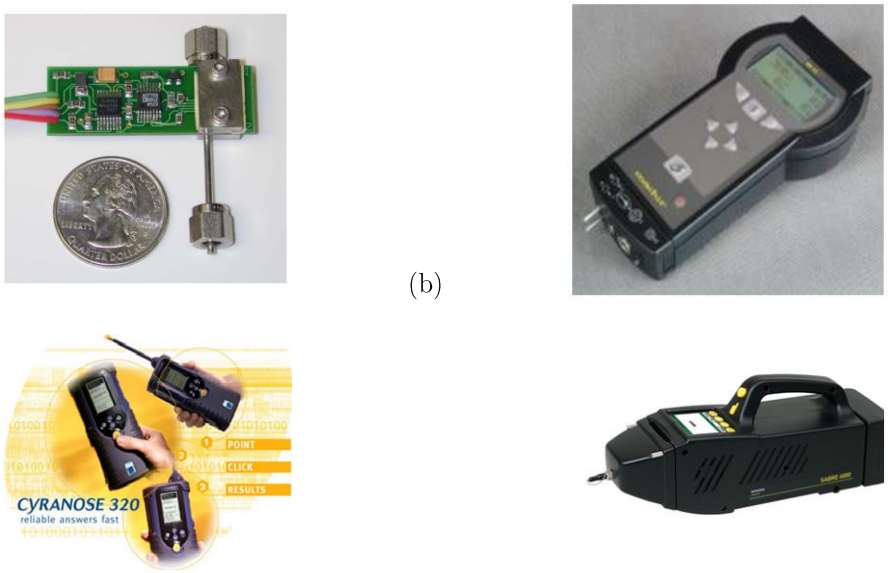


Figure I.2.3: Photography of some e-nose systems: (a) miniature sensor for dimethyl methyphosphate detection developed by the University of Tennessee [Pin07]; (b) GA-12plus portable gas analysers for the measurement of combustible gases produced by Madur [MAD]; (c) Cyranose 320 sensors dedicated to volatile organic compounds (VOCs) by Cyrano Sciences [CYR]; (d) SABRE 4000 detectors from Smiths Detection for chemical warfare agents (CWAs) and Toxic Industrial Chemicals (TICs) sensing [SMI].

II.1.2 – Mass spectrometers

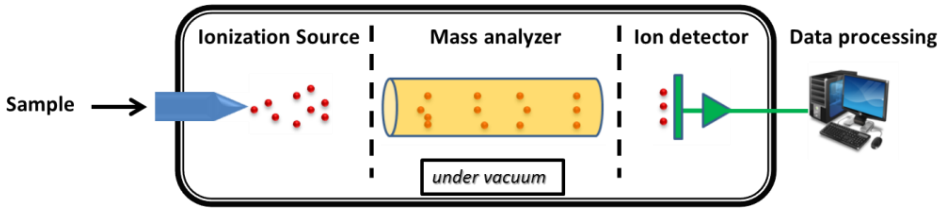


Figure I.2.4: Basic components of conventional mass spectrometry.

Mass Spectrometry (MS) is a universal technique to determine the chemical composition of a given liquid or gas substance. The MS principle of operation relies on the ionization of neutral analytes and on the measurement of the trajectories taken by the resulting charged particles in vacuum under electromagnetic field. Four stages compose such a device (depict in Figure I.2.4): an injection of vaporized sample stage, an ionization source which ionizes the particles, a mass analyzer which sorts the analytes according to their mass-to-charge; or m/z ratio, and an ion detector. After data processing, the molecular weight of each element composing the mixture is analyzed from their m/z ratio thanks to a spectrum analyzer.

It is widely used in a broad range of domains such as medicine, biology, pharmacology, material science, chemistry, geology, from the carbon dating to the detection of pesticides traces for instance. We tend now to extend the use of MS in the proteomics field. The latter corresponds to the analysis of biomolecules, e.g. proteins, macromolecular complexes, viruses, bacteria etc.

According to Figure I.2.5, MS is able to detect and measure the amount of low mass particles, but have difficulties for bigger one over than 100kDa (kilo Dalton[5]) corresponding to the mass of these biomolecules. Indeed, the measurement in this range requires large electromagnetic fields. Furthermore, this apparatus suffers from a poor resolution for this mass range.

As said before, this technique is based on the charge of the samples, which requires of ionizing the species. On one hand, this step can destroy the elements or modify their properties, and on the other hand the neutral particles cannot be measured. All of this lead to a loss of information and constitute the main drawbacks of standard MS. The use of NEMS-based device could solve both the problem of biomolecules detection and the measurement of neutral species without any ionization step [Sag13].

[5]The Dalton (or Da) is a measured unit used for the mass detection. One Dalton corresponds to the mass of the proton, *i.e.* 1.67×10^{-27}g.

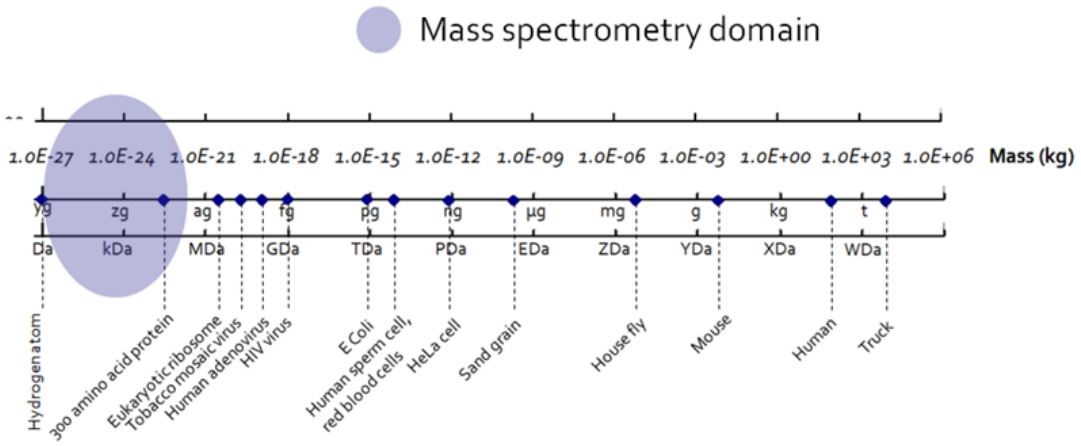


Figure I.2.5: Conventional Mass Spectrometry masse range, orders of magnitude [Hen12].

II.2 NEMS resonators as mass detection sensor

The working principle of mass sensing with NEMS resonators is based upon the study of the evolution of its resonant frequency over time. This electromechanical system can be modelled by a mechanical spring with a stiffness coefficient k and a total mass M. The expression of the mechanical resonance frequency $f_0$is given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{M}} \tag{I.1}$$

In the context of mass detection application, the resonant structure is directly in interaction with its environment. If a minute mass Δm (compared to the mass of the mechanical structure) is adsorbed at the surface of the system, a shift of the resonant frequency occurs, as explained in the following equations:

$$f = \frac{1}{2\pi}\sqrt{\frac{k}{M+\Delta m}} = \frac{1}{2\pi}\sqrt{\frac{k}{M}}\cdot\left(1+\frac{\Delta m}{M}\right)^{-\frac{1}{2}} \tag{I.2}$$

Since $\Delta m << M$, a Taylor expansion can be used to obtain:

$$f \approx \frac{1}{2\pi}\sqrt{\frac{k}{M}}\cdot\left(1-\frac{1}{2}\cdot\frac{\Delta m}{M}\right) \approx f_0 - \frac{1}{2}\cdot\frac{\Delta m}{M}\cdot f_0 \approx f_0 - \Delta f \tag{I.3}$$

$$\Delta f \approx \frac{\Delta m}{2M}\cdot f_0 \tag{I.4}$$

The frequency shift Δf is proportional to the mass Δm present on the beam. By following the evolution of the frequency shift over time, a mass sensor can be implemented (see Figure I.2.6).

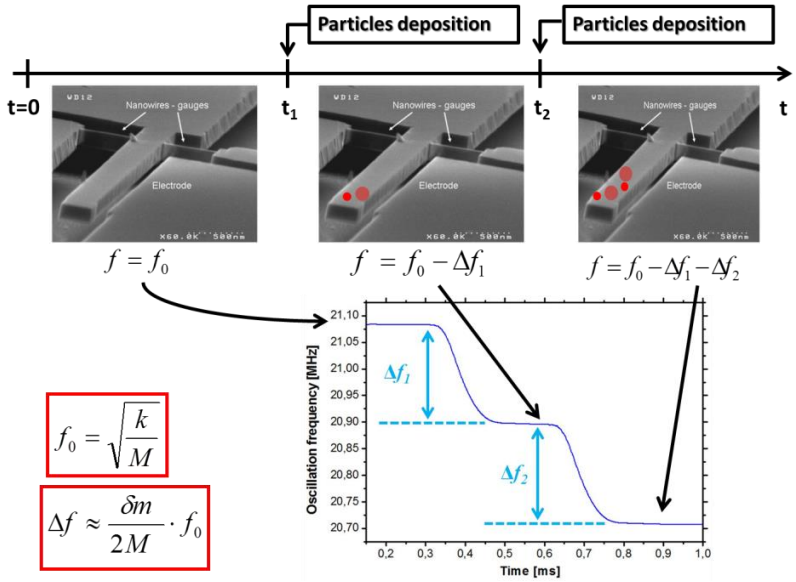


Figure I.2.6: Schematic explanation of a resonator used as mass sensor. The study of the mechanical resonance frequency evolution over time is performed. Each frequency shift is directly proportional to the mass deposited on the resonant structure.

Two major notions are used to characterize the performance of a mass sensor: the sensitivity and the mass resolution. The sensitivity *R*corresponds to the variation of the resonance frequency f_0 in respect to the mass m deposited on the movable structure. This sensitivity shows how the system reacts under a small perturbation due to a mass variation. The mass resolution δm is by definition the minimum quantity detectable by the sensor. Equations (I.5) and (I.6) define these two notions and show that R and δm depend on the mechanical resonance frequency f_0, the resonator mass M, the quality factor Q, the dynamic range of the sensor DR. These notions will be more explained in chapter II. L stands for NEMS length.

$$R = -\frac{\partial f_0}{\partial m} = \frac{f_0}{2M} \propto L^{-4} \qquad [\mathrm{Hz.kg^{-1}}] \qquad \text{(I.5)}$$

$$\delta m = \frac{M}{Q} \cdot 10^{-\frac{DR}{20}} \propto L^3 \qquad [\mathrm{kg}] \qquad \text{(I.6)}$$

This overview on gas sensors and mass spectrometers presented in II.1.1 and II.1.2allows emphasizing some major criteria defining a high performance mass detector:

- an easy miniaturization requiring few steps and few requirements;
- a low-cost production;
- a low power consumption;
- a fast response time;
- a high level of sensitivity;
- anda low level of resolution.

M/NEMS resonators fulfill all these criteria. They contain three major parts: a movable and released structure (generally a beam), an actuation and a transduction means. The released structure constitutes the sensing part and is set into motion by the actuation part. The transduction part converts then the mechanical displacement of the cantilever into an electrical signal which can be treated by an electronic circuit. Such devices are mainly fabricated following a top-down approach by using the surface and bulk micromachining processes. Various actuation strategies exist in the state-of-the-art (optical [Ver07]; magnetic [Hua03]; electrostatic [Tru07]; thermo-elastic [Bar07], piezoelectric [Mas07]), as well as transduction strategy (magneto-motive [Cle96]; capacitive [Arc12], piezo-resistive [Oll12]).

Many developments of M/NEMS-based mass detectors have been reported in the literature. Lange's team from the Physical Electronics Laboratory of the ETH Zürich reported in 2002 the creation of a VOCs gas sensor made up of a resonant cantilever co-integrated with an on-chip CMOS circuit (Figure I.2.7). This laboratory shows that the performance of cantilever-based sensors in terms of limit of detection is comparable to other existing acoustic sensor dedicated to VCOs detection.

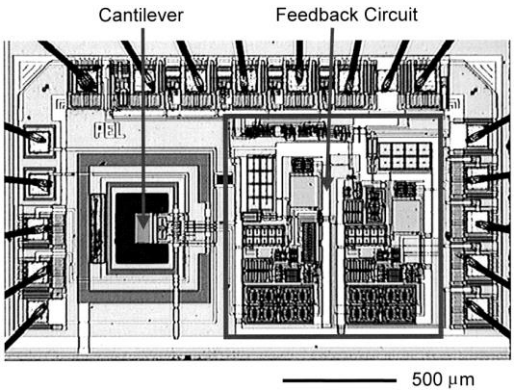


Figure I.2.7: Micrograph of the MEMS cantilever co-integrated with the feedback CMOS circuit [Lan02].

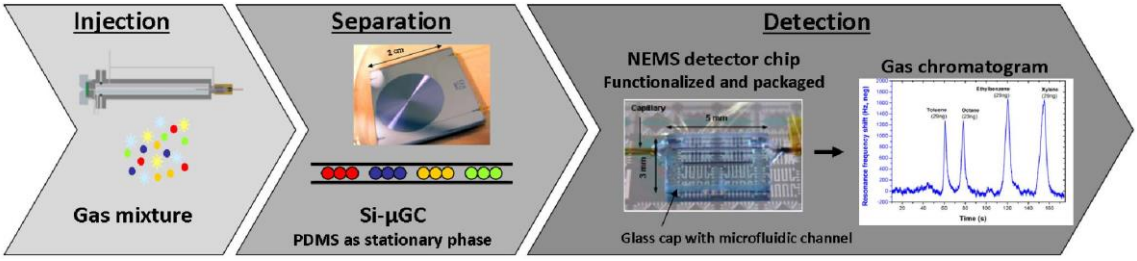


Figure I.2.8: Schematic representation of the multi-gas sensor composed of a micro gas-chromatography column for the separation stage and a NEMS resonator for the detection [Arc11].

Arcamone *et al.* have reported on a multi-gas sensor associating the use of a micro gas-chromatography column that separates the gas components and a NEMS resonator for a quantitative measurement. A schematic of this system is illustrated in Figure I.2.8. The determination of volatile organic compounds inside a gas mixture was demonstrated with a limit of detection of 2ag (one attogram corresponds to 1.10^{-18}g).

First experiments on mass resolution of NEMS resonators were performed in 2002 by the group of Prof. Roukes [Eki04]. Using a clamped-clamped SiC beam, a real-time detection with a mass resolution of 2.53ag was achieved. After that, other systems with better mass resolution were performed. The current mass record is held by the team of Bachtold that demonstrated a close-to ym resolution (one yoctogram corresponds to 1.10^{-24}g, *i.e.* the mass of a hydrogen atom) with a Carbon Nanotube resonant structure [Cha12]. The first NEMS-MS experimental demonstration is reported in [Nai09] in which a 17zg resolution system is developed.

II.3 M/NEMS implementation issues

In order to have a high performance mass detector, high sensitivity and low resolution are required. From (I.5) and (I.6), R and δm seem to be linked to the length of the mechanical resonator. So, by scaling down the dimensions of the resonant structure, a drastic improvement of the sensitivity and resolution is possible, as described in Figure I.2.9.

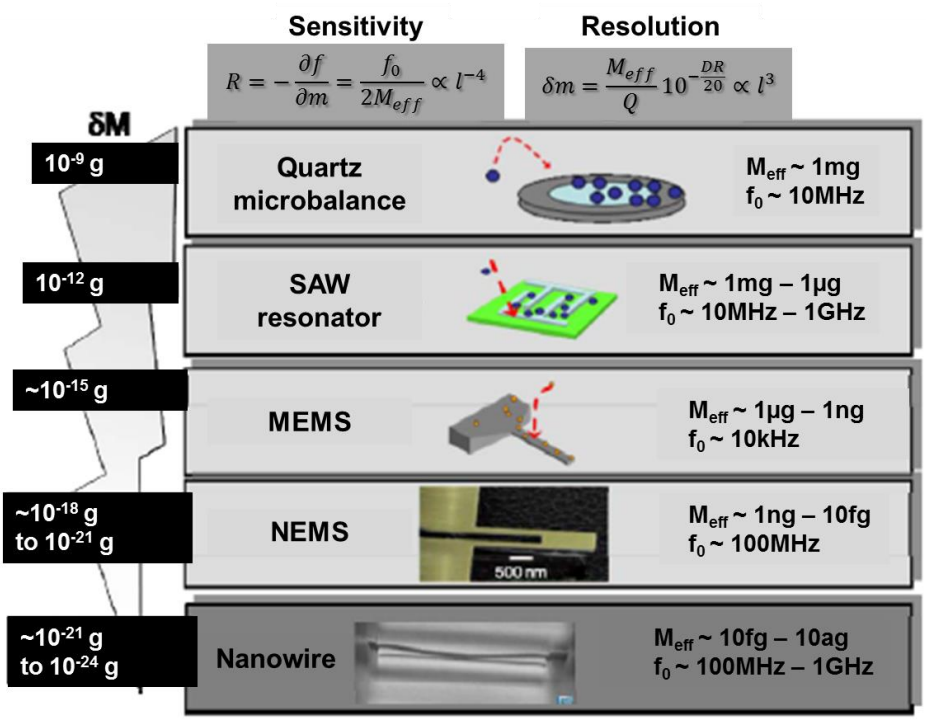


Figure I.2.9: Variation of resonance frequency and mass resolution with MEMS dimension decrease.

References	**[Eki04]**	**[Yan06]**	**[Chi08]**	**[Cha12]**
L (µm)	10	2.3	0.4	0.150
f_0 (MHz)	72	133	300	1862
R (MHz/pg[6])	2.56	890	$9.3x10^7$	$3.1x10^{12}$
δm (ag[7])	2.53	$7x10^{-3}$	$85x10^{-6}$	$1.7x10^{-6}$

Table I.1: Illustration of the sensitivity and mass resolution improvement with the decrease of the resonator dimensions.

The improvement of these characteristics is demonstrated in the Table I.1 which depicts and compares the performance of some systems. In consequence, this improvement requires a transition from MEMS to NEMS resonators. In order to increase the capture area to collect the largest number of molecules and to increase the precision, these NEMS can be arranged in arrays by VLSI integration (as shown in Figure I.2.10).

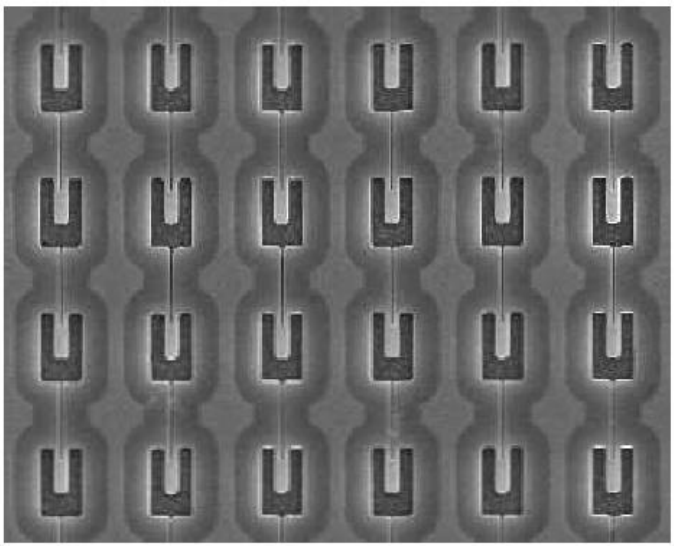
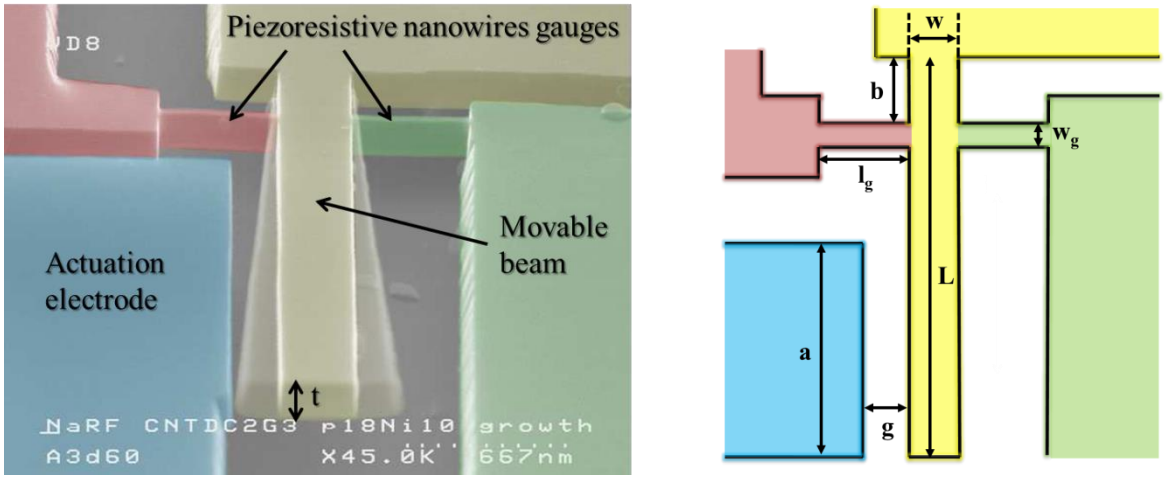


Figure I.2.10: Example of NEMS resonators arranged in an array [Arl11].

[6]A picogram (or pg) corresponds to 1.10^{-12}g.

[7] An attogram (or ag) corresponds to 1.10^{-18}g.

Furthermore this dimension reduction leads to another issue. Indeed, the smaller the electromechanical system is, the smaller the beam displacement is. Thetransduction scheme needs to be selected carefully in order to detect slight displacements of the cantilever. For both gas sensing and MS, a NEMS resonator made up of single-crystal silicon (c-Si) with an electrostatic actuation and a piezo-resistive transduction constitutes an efficient solution. The actuation stage converts a voltage into an electrostatic force and the transduction scheme converts a mechanical stress due to the beam displacement into an electrical signal thanks to two piezo-resistive nanowires gauges. This structure is also called "crossbeam" and is illustrated in Figure I.2.11 [Mil10]. C-Si appears as an excellent candidate as structural material since it provides a high piezo-resistive gauge factor [Bar09]. On the other hand, these structures are very interesting because of their low-cost production and their compatibility with CMOS technology, which may lead to VLSI development optimum for the NEMS arrays implementation and a possible co-integration with CMOS circuits.



Beam length	Beam width	Gap electrode/beam	Gauge length	Gauge width	Electrode length	Anchor/gauge distance	Beam thickness
L	W	g	l_g	w_g	a	b	t
~5µm	~300nm	~200nm	~500nm	~80nm	~3.5µm	~750nm	~160nm

Figure I.2.11: Artificially colored and modified SEM image illustrating the "crossbeam" resonator structure (on the left) [Mil10] and presentation of its geometric dimensions (on the right). The table below indicates typical values for these dimensions. The miniaturization of the crossbeam structure can concern all of these geometric parameters.

III. M/NEMS-CMOS integration

The beginning of section II.2 explained the use of M/NEMS resonator as mass sensor. The study of the resonance frequency evolution over time allows the determination of the amount of molecules adsorbed by the mechanical cantilever. This requires the tracking of this frequency in real-time by operating the NEMS in close-loop. However, this close-loop implementation is impossible with a NEMS alone and a feedback is necessary. This feedback may be played by an electronic circuit fabricated using CMOS technology. This circuit is used both as a readout system and as a way to put the mechanical structure into oscillation. For the fabrication of mass sensor, the NEMS-CMOS integration process has to be carefully selected, and particularly the way to interconnect the sensing part with the circuit. There are two main strategies to integrate these two blocks together in order to make the sensor: the hybrid and the monolithic approach (Figure I.3.1). These two schemes are explained in the following paragraphs.

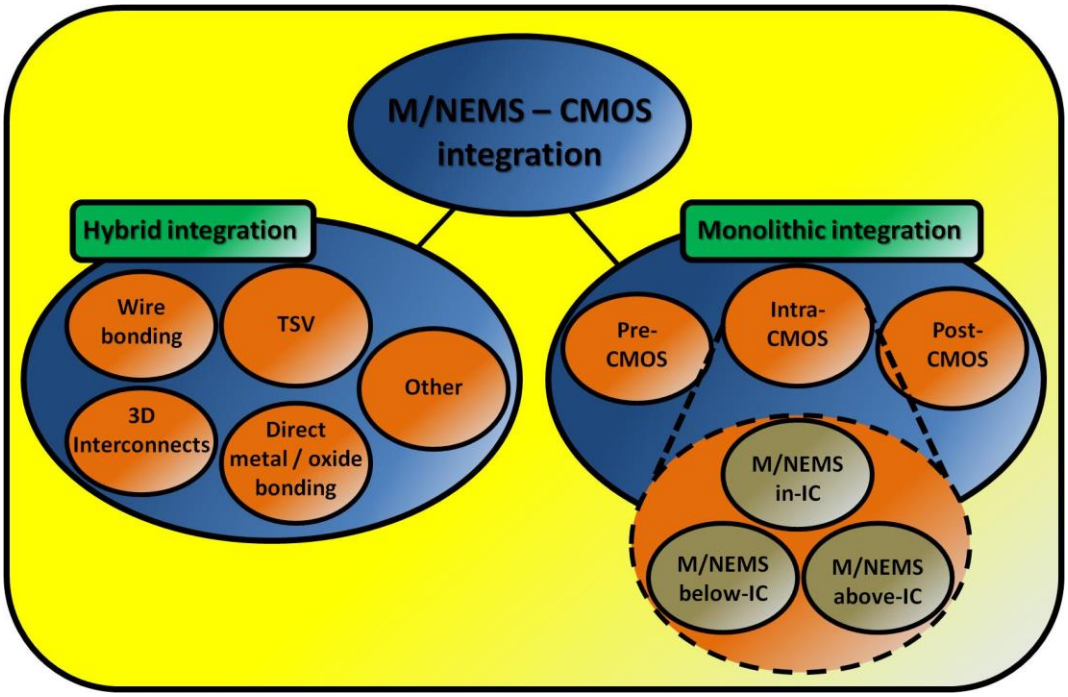
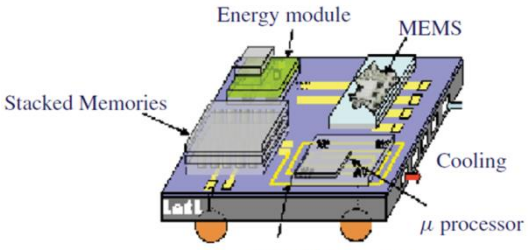


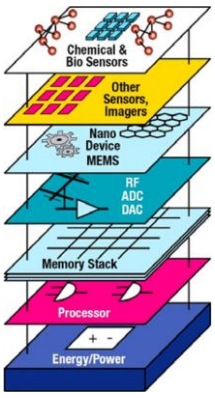
Figure I.3.1: Diagram representing the different integration technologies between M/NEMS devices and CMOS circuits. Two major types of integrations are possible: hybrid and monolithic integration. Within monolithic integration, there are three main types: MNEMS below-IC, in-IC and above-IC.

III.1 Hybrid integration

This approach consists in integrating different functions, e.g. stacked memory, digital processing, energy module, sensing part and so on in the same package (as illustrated in Figure I.3.2). It is a promising alternative to the classical and most used method where the components are individually packaged and laterally assembled on a board such as printed circuit board (PCB). The main goal of this scheme is to manufacture a multi-functional chip. This strategy is also called System-in-Package (SiP), or stand-alone approach, and uses a parallel integration way: all the elements are processed on separate dies, and are connected together at the end of the process. As a consequence, every element can be fabricated without impacting on the fabrication of the other one. Several options of hybrid integration exist according to the disposition of the M/NEMS part in respect to the CMOS part (2D or 3D), and the way to interconnect them together [Gar08]. In 3D integration, the assembly can occur at different scale: wafer-to-wafer (W2W), die-to-wafer (D2W) or die-to-die (D2D). The following paragraphs will make an overview of the existing solutions: wire-bonding, 3D interconnects, direct metal-oxide bonding, TSV and other options.



(a)



(b)

Figure I.3.2: Representation of a multi-functional chip fabricated with a hybrid integration scheme using both 2D and 3D approaches (a) [Sou11] and a 3D approach presenting a "3D hyper-integration"(b) [Lu09].

III.1.1 – Wire bonding

Wire bonding is a classical approach which consists in interconnecting the metal pads of two different chips by a wire, as shown in Figure I.3.3. This technique uses a ten or hundred micron size metal wire, made generally in gold (Au), silver (Ag) or aluminum (Al) [Geh80]. It allows both a 2D and 3D integration. This technique presents a lot of advantages compared to traditional assembly on PCB: the process is compatible with CMOS (temperature inferior to the thermal budget limit of the interconnection), a low alignment precision is required because of the pad size and pitch between each other (~50µm minimum for both size and pitch [Qin02]), and the bonded-wires have a low electrical resistance (from 1 to 100mΩ). However, this technique introduces strong signal attenuations due to high parasitic capacitance generated which can reach 10pF [Arn11].

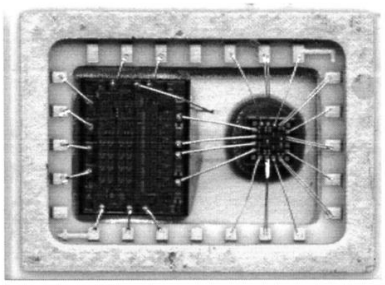
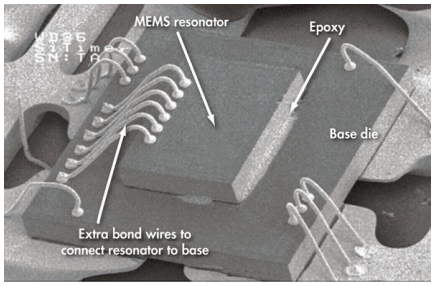
(a)  (b) 

Figure I.3.3: Wire bonding between RF-MEMS and CMOS circuit in 2D (a) [Sil03] and 3D configuration (b) [Pet13]

III.1.2 –3D interconnects for "flip-chip" assembly

This section will focus on the way to interconnect two substrates in parallel through some local 3D interconnects such as micro-insert [Wat10], micro-tubes [Mar13], micro-bumps [Mil69-Che09], Transient Liquid Phase (TLP) interconnects [Col13] etc. [Lau11-Lam13]. Some of them are shown on Figure I.3.4. The integration here consists in processing both CMOS and NEMS on separate dies. Then, on one of these two substrates (wafer or chip) are fabricated the interconnect elements. On the other substrate are build pads where the connection will be performed (see Figure I.3.5). The final assembly generally used a thermo-compressive process until 400°C to respect the compatibility with CMOS technology. More details about the process flows can be found in [Lam13] and [Col13]. An example of such MEMS-CMOS integration was performed in 2001 by the team of C. T. C Nguyen [Won01]. This team demonstrated an integration of a RF MEMS assembled on a CMOS circuit using micro-bump interconnects, as illustrated on Figures I.3.6 and I.3.7.

Like wire-bonding, this technique allows the process of one part (sensing or electronic) without affecting the fabrication of the other one. Typical dimensions of these elements are weak (between 1 and 10µm of diameter and length), allowing thereby a low electrical resistance (between 10 to 100mΩ) [Col13]. Furthermore, the electrical signal is less attenuated than in wire bonding case. Indeed, no strong capacitance is introduced with this method. Another advantage is the considerable gain in area compared to the previous technique in 2D integration case. However, this process requires a lot of fabrication steps and a careful attention during the assembly, more particularly on the alignment of the substrates. Furthermore, all of these technologies have a minimum pitch corresponding to the minimal distance between two interconnects (10µm minimum). These interconnects impose the minimum distance between two M/NEMS devices and thereby the density of NEMS arrays. Another major drawback is the throughput of this strategy: W2W integration is difficult and sometime impossible for some of these interconnect elements [Gou11].

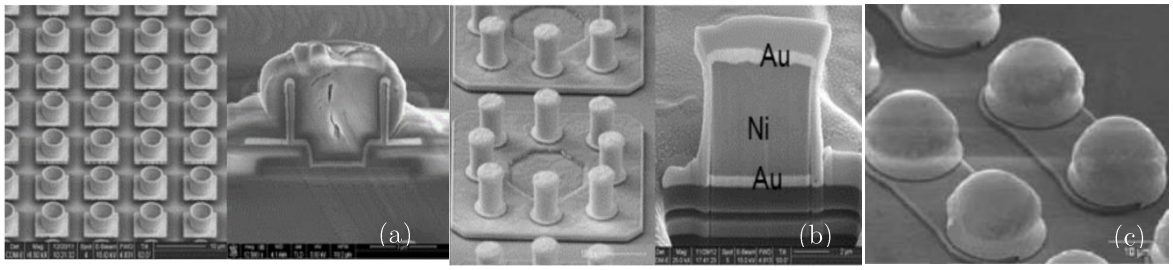


Figure I.3.4: SEM and FIB micrographs of micro-tubes (a) [Col13], micro-inserts (b) [Col13] and micro-bumps (c) [Lau11].

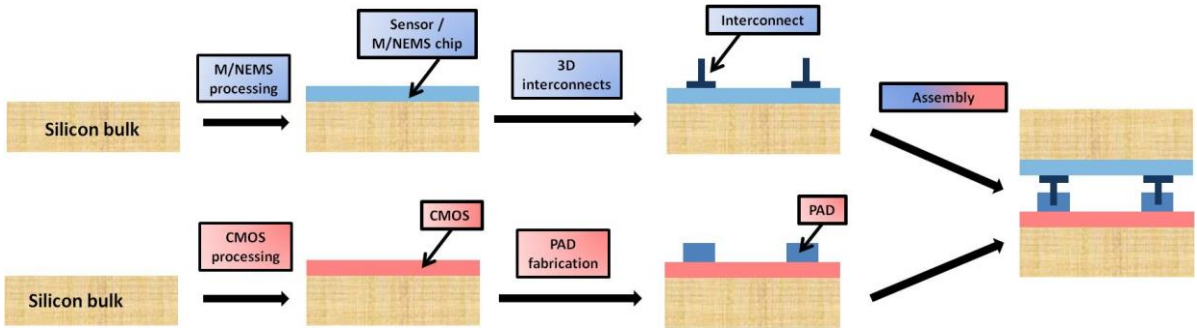


Figure I.3.5: Schematic representation of the process flow of 3D interconnection technology for a "flip-chip" assembly. Both the CMOS and the M/NEMS parts are processed on separate dies first, then 3D interconnects and pads are respectively manufactured on sensor and electronic substrates. A thermo-compressing step may or not be necessary according to the 3D interconnection strategy used.

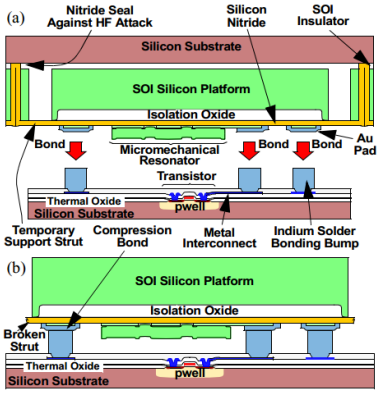


Figure I.3.6: (a) Schematic cross-section of the MEMS-CMOS assembly process using micro bump leading to the final results (b) [Won01].

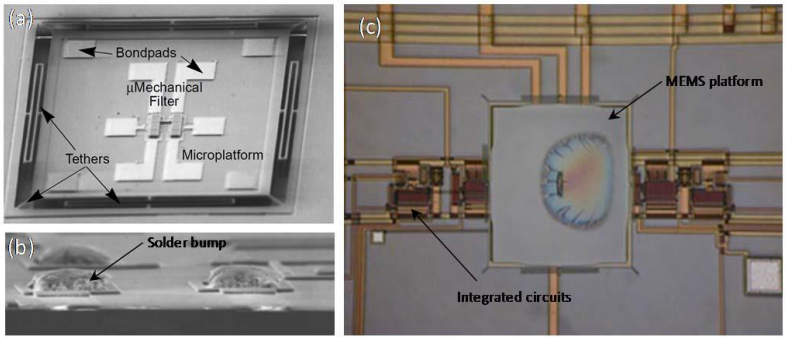


Figure I.3.7: SEM micrographs (a) showing the electromechanical device with embedded bond pads. (b) a zoom on the solder bumps placed on the electronic substrate. In (c) is shown a view of the RF MEMS device placed on the electronic substrate [Won01].

III.1.3 – Direct metal-oxide bonding

Metal-oxide bonding techniques allow both the bonding and the connection between the electronic and the sensor substrates at the same time. The metals commonly used for this connection are copper (Cu), gold (Au), tin (Sn) and lead (Pb) [Ko10]. Several bonding techniques can be used for this approach [Cio11] although their principle is more or less the same. Like previous approaches, this technique allows the fabrication of the CMOS and the M/NEMS devices without impacting both elaboration processes, from the device to the interconnection manufacture. Then the assembly and electrical connection is performed by direct bonding. Several options are possible depending on the bonding process (Figure I.3.8). The first possibility consists in performing a blanket deposition of oxide (generally SiO_2) at the surface of the substrates followed by an oxide bonding. A metal layer deposited near the bonding interface and before the bonding process is necessary for the connection between the substrates (Figure I.3.8 (a) and (b)). Another possibility consists in depositing at the surface of the substrates both the oxide and the patterned metal and to proceed to a hybrid direct bonding (Figure I.3.8 (c)). A simplified process flow is described in Figure I.3.9. In some cases, the bonding may be performed or not by a thermo-compression technique that may damage devices. Like the previous technique, this one is processed at a temperature up to 400°C respecting the CMOS compatibility. Furthermore, the hybrid oxide metal bonding is based on the inter-diffusion of metal atoms which offers a better contact than 3D interconnects approach (around 10mΩ per contact [Cio11]). The minimum pitch achievable here is interesting (<10µm [Bei13]) and can be smaller than the one obtained with 3D interconnects. No parasitic capacitance is introduced with this technique.

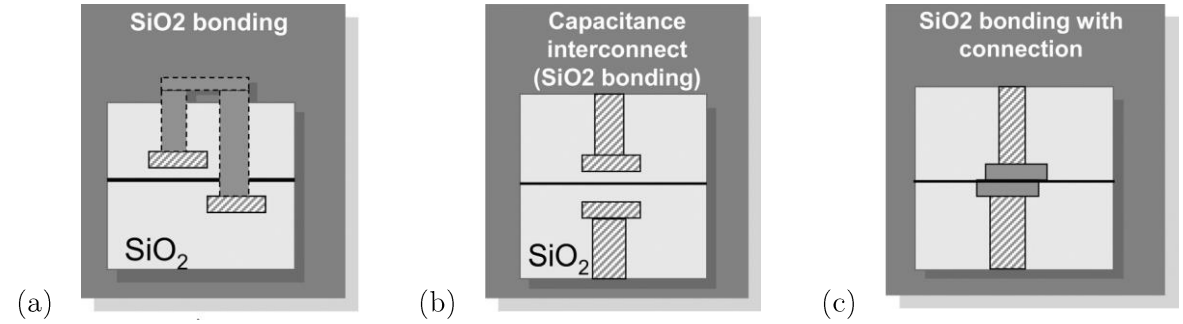


Figure I.3.8: Cross-sectional schematic representations of different direct bonding options: direct oxide bonding for a resistive (a) or capacitive (b) interconnection; direct oxide metal bonding (c). The hatched and dark forms represent metal layers [Cio11].

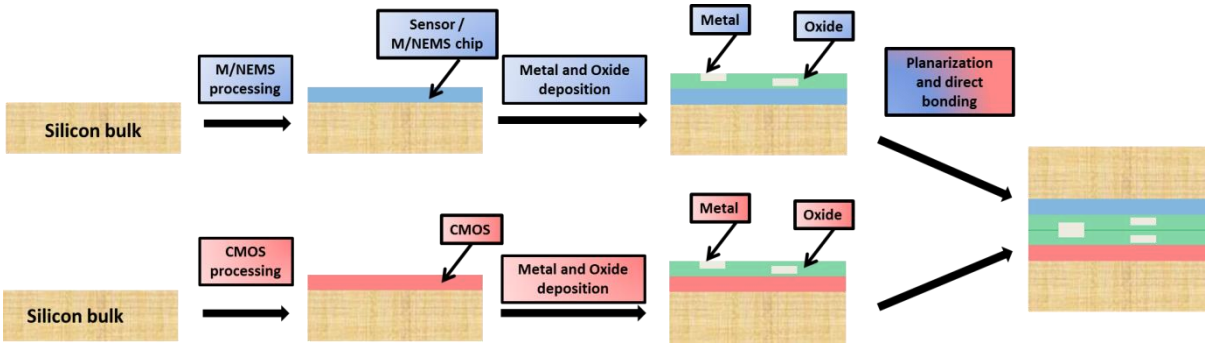


Figure I.3.9:Schematic representations of the process flow using a direct bonding process. Both the CMOS and the M/NEMS parts are first processed on separate dies. After the interconnection fabrication, both metal and silicon oxides are deposited, and a surface planarization is performed, followed by the bonding step.

Moreover, this technique allows W2W integration and a higher throughput in respect to the previous technique. However, its implementation requires many precautions for the bonding step. Indeed, oxide surfaces on the two substrates must be very clean without any presence of particles. The topography is another key parameter and has to be as low as possible after planarization (few nanometers). As metal patterns are present near the surface of the substrates, the alignment is also very important during the process. A misalignment can lead to some electrical contact problems and also to a local delamination in oxide-metal interface [Gue10]. A MEMS-CMOS stack following such strategy was studied by the group of C. S. Tan from the Nanyang Technological University in Singapore [Nap12]. The particularity of this study is that the CMOS substrate plays the role of encapsulation and is bonded on the MEMS-based accelerometer substrate (Figure I.3.10).

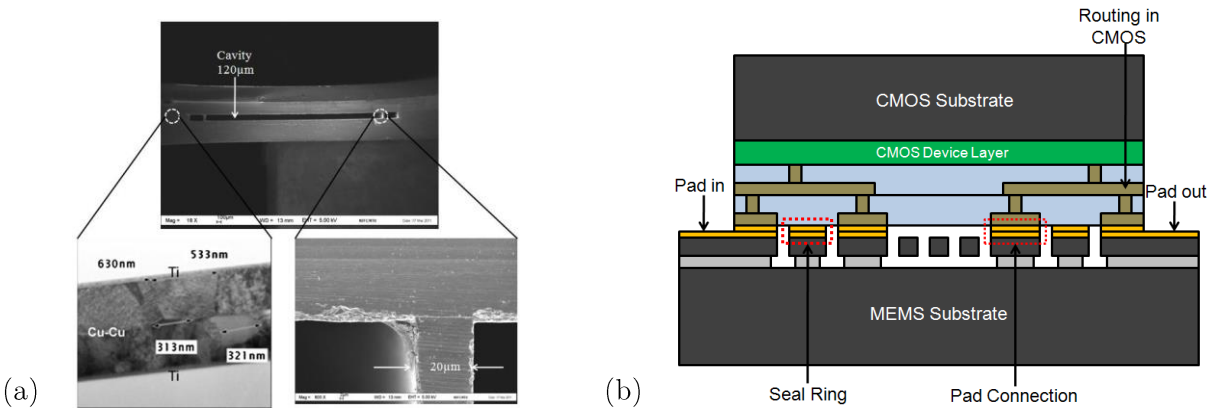


Figure I.3.10: SEM Micrograph of Cu-Cu bonding (a) and schematic cross-section of the MEMS-CMOS device with a CMOS substrate as encapsulation (b). The direct bonding is performed at Cu level (represented in yellow here) [Nap12].

III.1.4 – Through Silicon Via technology

Through Silicon Vias, also called TSVs, correspond to wide and long vertical metallic interconnects used for 3D integration and chip stacking. TSVs allow electrically connecting two chips through silicon bulk thanks to a high aspect ratio via[8]. A thinning step of silicon substrate is also used to limit via length. Several technological strategies can be found for TSVs integration (explained in Figure I.3.11). Each strategy uses different process temperatures and imposes different constraints on the dimensions and filling materials of TSVs. Here is exposed a basic description of each option.

The so-called "Via First" approach is done before the device fabrication and allows very high aspect ratio (superior to 8) vias without any temperature limitations. The silicon bulk substrate thinning step is processed after via filling. However, best electrical conductive materials such as Cu and Al are forbidden to fill TSVs in order not to affect subsequent process tools by contamination and not to damage the electronic devices. These materials are replaced by other compatible ones such as polycrystalline silicon (poly-Si) and tungsten (W). Nevertheless, their conductivity property is worse than Cu and Al, making this via first approach very little used.

In the "Via Middle" process, TSVs are fabricated just after the device and before the interconnections or just after the first metal interconnection layer (M1). In this strategy, Cu can be used for filling vias with a diameter between 3 and 20µm and a depth between 50 and 150µm. A thinning step is finally performed at the end of the process. The maximum thermal budget limit here is imposed by the metal interconnection layer (near 450°C) if TSVs are made after the M1 layer.

[8] Aspect ratio corresponds to the ratio of the length over the width of a via.

The “Via Last” approach consists in building both the etching and filling steps after interconnection creation. This TSVs manufacture can occur before or after substrate thinning. The latter requires for all approaches a bonding of the top face to a handling carrier. The thermal budget limit for the via last strategy is imposed either by the interconnection metal or by the glue used for the bonding respectively if the substrate thinning occurs after or before TSVs building. In the second case, the maximum temperature allowed is 250°C for all the process. For both “Via Middle” and “Via Last” process, a barrier material deposition (*i.e.* titanium nitride or TiN) is first deposited after the TSVs etching in order to prevent from the diffusion of Cu in silicon.

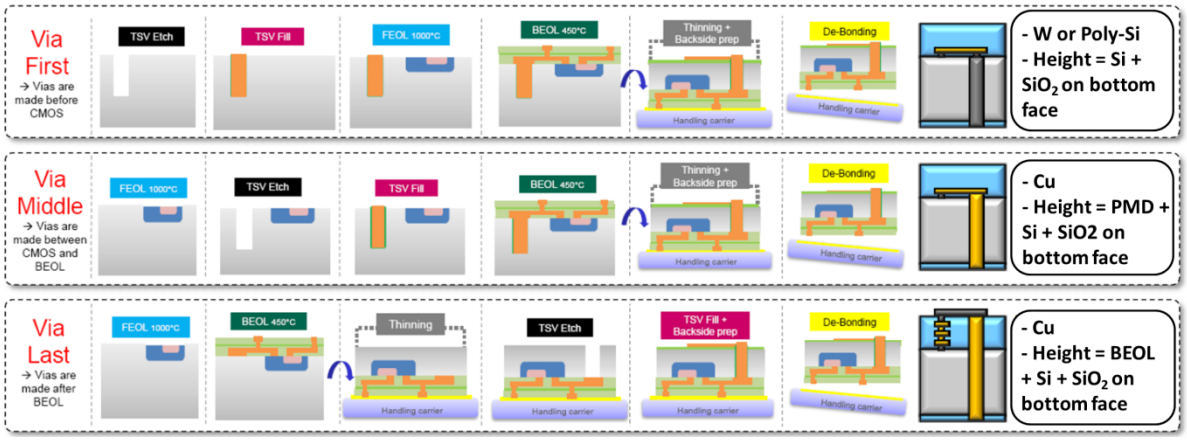


Figure I.3.11: Schematic of the three different strategies for TSVs integration (with CMOS transistors as devices). PMD stands for Pre Metal Dielectric and corresponds to the oxide deposited after the device fabrication and before metallic interconnections creation [Bro2013]. BEOL means Back-End Of Line and will be explained more precisely in the next section.

To implement a 3D stack, the TSV process can occur either before or after the bonding of the different substrates. The latter can be a direct oxide or a direct metal-oxide bonding (see Figure I.3.12). As a consequence, the advantages and drawbacks described in the previous section are the same. Furthermore, unlike the direct bonding method, this technique allows to keep the M/NEMS devices in direct contact with the environment (no encapsulation). This parameter is very important for the mass sensing activity. However, this interconnection way introduces strong capacitances near 100fF [Cad11-Lee14], which can lead to a stronger signal attenuation than the integration schemes depicted in sections III.2 and III.3. Another major problem is the pitch between these 3D interconnections. The current state-of-the-art features diameter down to 2µm and pitch down to 10µm [Fra10]. Nevertheless, a particular area called “Keep-Out-Zone”, or KOZ, in which the electronic and mechanical properties of silicon change due to vias fabrication, creates strong mechanical stress on the active device layer around the TSV. The implementation of functional components is therefore not recommended in these areas. Electronically

speaking, the KOZ can be defined as the region with a change of carrier mobility over 5% [Ryu12]. Even if some solutions have been investigated to limit the KOZ [Sai14-Rab14-Wan14], its dimension is located between 5-10µm [Mer10-Bey12-Guo12] around the TSV and has to be taken intoaccount during functional devices fabrication, more particularly for NEMS array development.

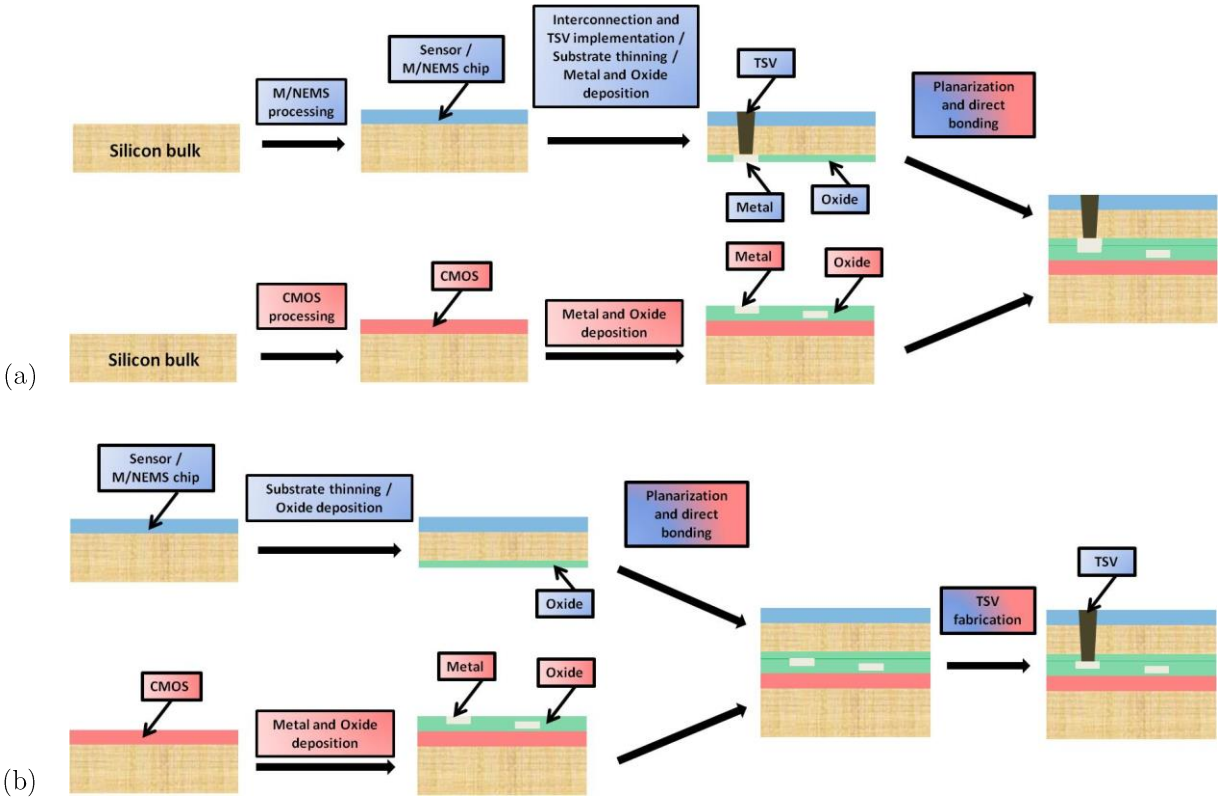


Figure I.3.12:Schematic representation of the process flow using TSV connection performed before (a) and after (b) the bonding. Both the CMOS and the M/NEMS parts are first processed on separate dies. The thinning here is applied on sensing substrate to allow a shorter and easier TSV fabrication. In (a) is depicted the case of direct metal-oxide bonding, but 3D interconnects can also constitute another assembly alternative.

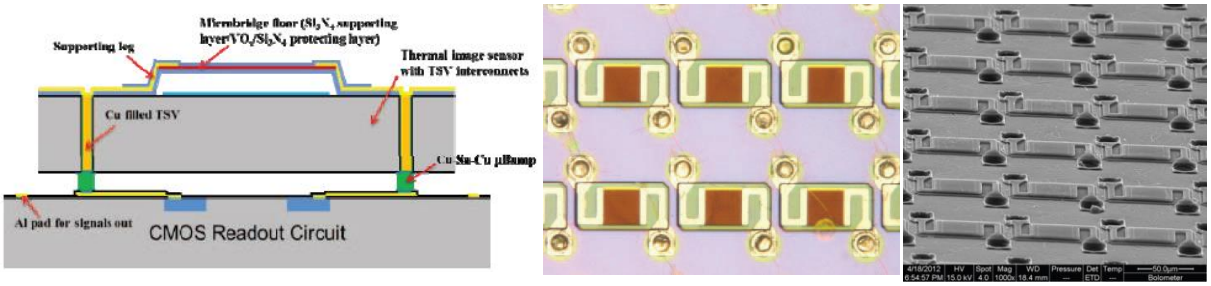


Figure I.3.13: Schematic cross-section (left) of a MEMS-CMOS sensor; optical microscopy and SEM view (respectively middle and right) of the MEMS array [Wan12].

Figure I.3.13 shows one MEMS-CMOS bolometer implemented using TSVs as interconnects with a 24µm diameter and a 98µm depth [Wa12]. A "Via-First" process is performed on the sensing wafer followed by the MEMS array fabrication. Substrate thinning is followed by bonding with the CMOS substrate using Cu/Sn micro-bumps. This bolometer system was designed for imaging applications.

III.1.5 – Other interconnect methods

The previous sections presented the most commonly used interconnect methods for a 3D hybrid integration scheme. Thereafter are reported two original 3D interconnect techniques for MEMS-CMOS integration. In 2010, Toshiba and Stanford presented a work on a concept of detachable nano-carbon chip [Fuj10]. NEMS is used here as a non-volatile switch and is made up of graphene. The electromechanical device is developed on a substrate with carbon nanotubes bundles as vertical interconnects. The stacking and electrical connection with other substrates is performed thanks to Van der Walls forces between carbon nanotube and metal pad without any adhesive material or adhering process, making this method attachable and detachable, as illustrated in Figure I.3.14. However, this work is only a concept without any experimental development published yet.

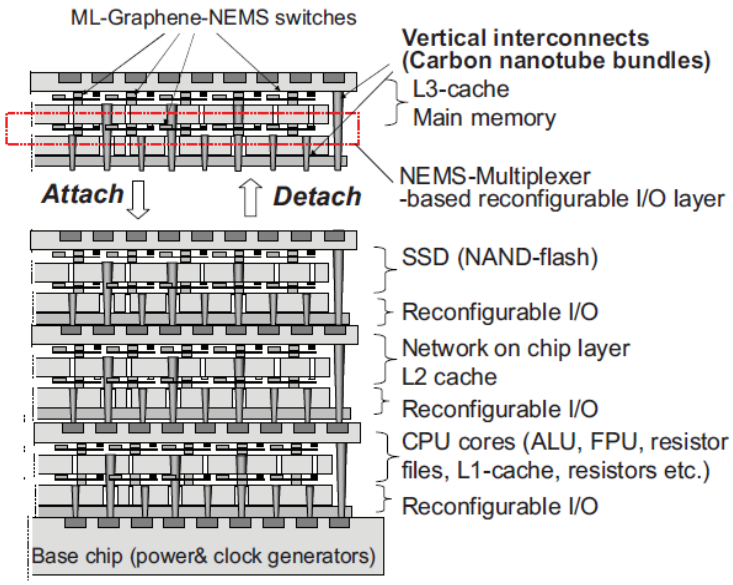


Figure I.3.14: Schematic representation of NEMS devices and the "attachable-detachable" assembly method using carbon nanotubes [Fuj10].

Another method was published in 2010 by the Gigascale integration group of the Georgia Institute of Technology. Yang *et al.* were able to integrate MEMS and CMOS using TSVs and a new kind of interconnects called Mechanically Flexible Interconnects or MFIs [Yan10]. These MFIs are made up of Cu and are fabricated at the surface of one substrate (the CMOS one in Figure I.3.15). To provide electrical connection, a polymer ring and a solder ball are deposited at the surface of these MFIs whereas pads are fabricated on the other substrate for the final assembly. Like the previous concept, this MFI-based technique does not need any direct bonding process which excludes any planarity requirements. This method is characterized by its huge flexibility. Indeed, both modules can be detached and reattached to other substrates, which can be useful for pre-test of devices before final assembly. However, in order to allow a direct interaction between the MEMS device and its environment, TSVs are necessary in the sensing substrate. As seen in the section III.3.4, this parameter can affect the density of electromechanical components.

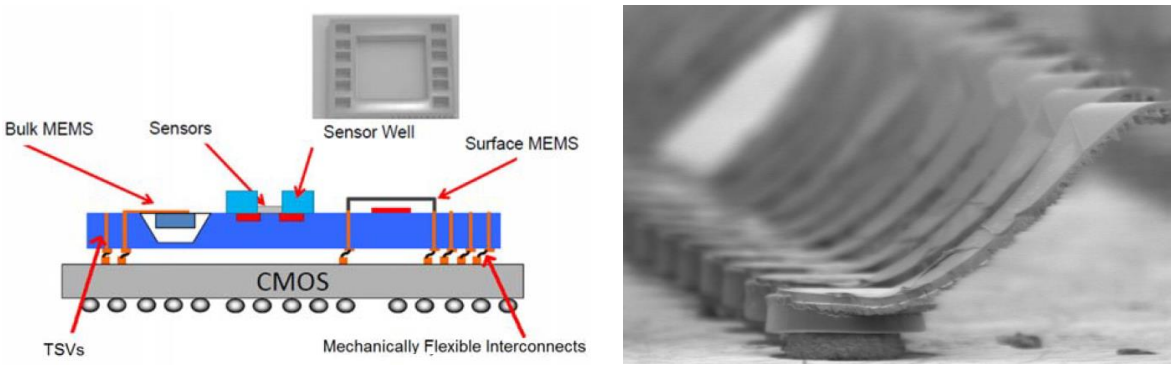


Figure I.3.15: Schematic representation of MEMS-CMOS integration using MFIs (on the left) and SEM side view of such interconnects (on the right) [Yan10].

A wide variety of hybrid integration techniques has been investigated in this part, illustrated with experimental implementations. For the selection of NEMS-based sensor fabrication, this approach must be balanced with the different possibilities offered by monolithic integration. The latter is addressed in the next section.

III.2 Monolithic integration

This integration scheme is the other alternative to integrate several functionalities on a same die. Monolithic integration consists in processing both the M/NEMS and the CMOS devices on the same substrate. Other terms are used to call this fabrication strategy, for example sequential or co-integration approach. This part will first focus on some definitions necessary for a better understanding. An overview of the different options will be presented through some experimental implementations with only M/NEMS resonators objects (and not other devices such as accelerometers, gyroscopes etc). After that, a comparison of all the strategies presented in this manuscript will be performed. This comparison will allow to select the presumably best scheme to implement a NEMS-based mass detector.

III.2.1 – CMOS stack description

A CMOS stack contains three main sections. The front-end of line or front-end zone (as known as FEOL or FE) corresponds to first fabrication steps of an electronic chip with the development of the functional devices, for example transistors, memories and so on. Then is build the middle-end (ME) in which is processed the contact. This level is also characterized by the deposition of some poly-Si layers. Finally is manufactured the back-end of line, or back end zone (BEOL, or BE) with the metallic interconnections which allow to drive and use the front-end devices. An illustration of this stack is shown on Figure I.3.16 with the specifications on the layers, the typical materials used, the standard maximum temperature supported by the levels and the consequences of a higher temperature exposition. This figure depicts a 2P6M CMOS stack with two poly-Si levels (2P) and six metal levels (6M). This notation will be used throughput this manuscript to describe CMOS interconnection technology. The CMOS process flow will not be detailed here[9].

[9]For more information, please refer to [Bra05].

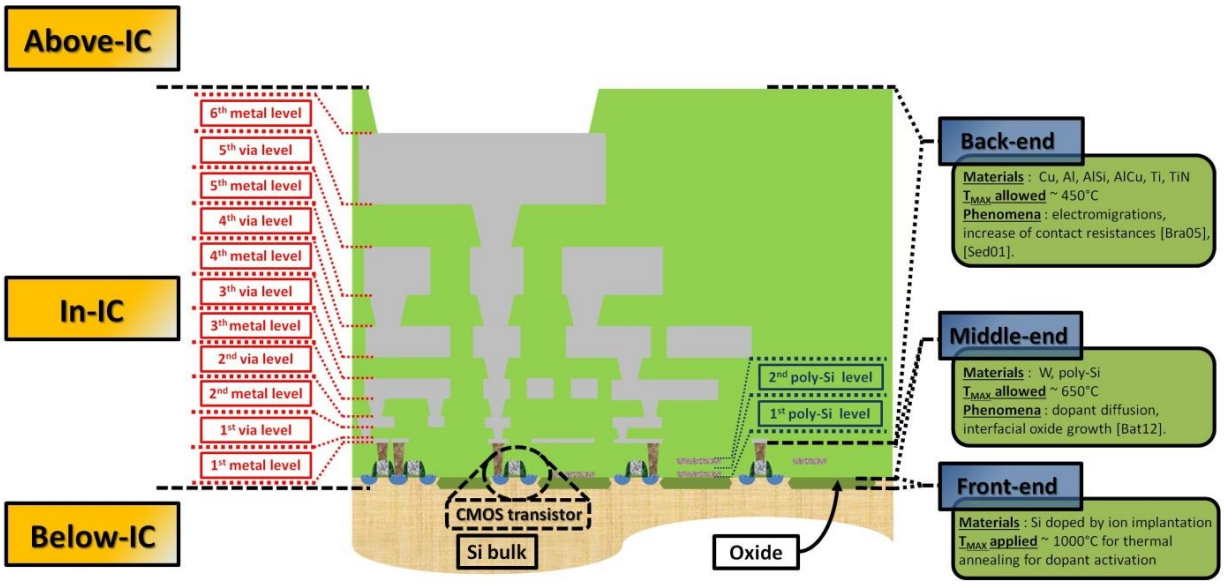


Figure I.3.16: Schematic cross-sectional view of an advanced CMOS stack from a standard foundry.

III.2.2 – M/NEMS implementation process

It is important to understand first the development of electromechanical resonators before the selection of a M/NEMS-CMOS integration strategy. This section proposes to briefly explain a typical process flow of NEMS resonator (Figure I.3.17). Such systems are usually performed on the single-crystal silicon (c-Si) layer of an SOI wafer (Silicon On Insulator). First of all, an ion implantation and a thermal annealing are performed in order to adequately dope the c-Si to tune the piezo-resistive gauge factor. Nature and dose of dopant for implantation step on the gauge factor value [Kan82-Smi54] and on the preferential crystalline orientation which maximize piezo-resistive effect. A p-type dopant such as boron is generally used and provides better coefficient than n-type. Examples of typical annealing temperatures and duration for dopant activation are 800°C for 30 min and 1050°C for 3 min. Then, resonators are patterned by lithography and etching operations. After that, a passivation layer is deposited on c-Si. All these steps define the FE level. The contact and interconnections are made by a metal deposition after pads aperture through the passivation. Finally, after lithography and etching of the metal layer, mechanical structures are then released by etching both passivation oxide and the BOX from the SOI substrate.

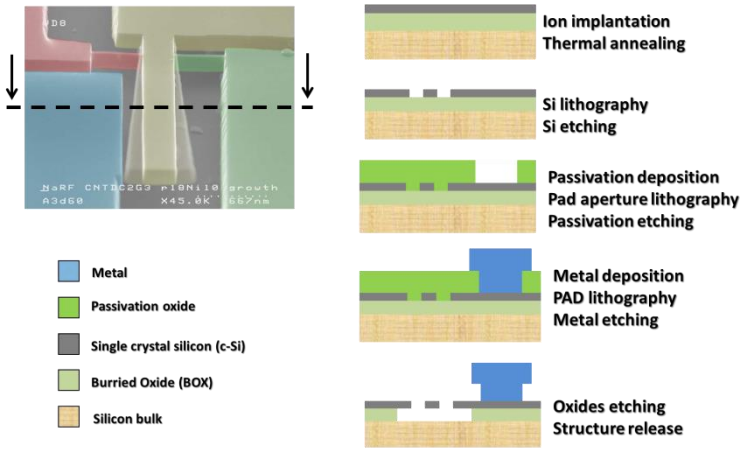


Figure I.3.17: Cross-sectional schematic of a commonly NEMS process flow.

III.2.3 – Pre, Intra or Post-CMOS fabrication

As described just before, NEMS fabrication uses some critical steps, such as thermal annealing, metal deposition and release. Such processes can be destructive for the CMOS and interconnect components. Thus, the choice of NEMS-CMOS co-integration strategy is critical. In this context, three different options exist, so-called pre-CMOS, intra-CMOS and post-CMOS.

The pre-CMOS or M/NEMS-first approach first consists in processing the M/NEMS devices before the CMOS transistors. Its main advantage is the possibility to use high-temperature processes without any thermal budget constraints, such as poly-Si deposition, thermal annealing for dopant activation or high-temperature etching. This strategy may require a modification of the CMOS fabrication process, what impacts the cost and may degrade the yield of the CMOS line.

In intra-CMOS or intermediate micromachining approach, the implementation of electromechanical systems occurs after CMOS devices and before the interconnections. It is commonly used to integrate poly-Si microstructures in CMOS technologies [Bra05]. Such an approach allows the use of high temperature steps below 650°C in order not to affect the doping profiles and the gate oxide [Bat12].

The post-CMOS option implies to fabricate M/NEMS devices after front-end and back-end steps. Due to the metallic interconnections, the process is limited to 400-500°C, for standard and low-cost Al and Cu based interconnection metal, prohibiting thereby high temperature steps such as LPCVD deposition and thermal annealing. This approach is flexible: front-end and back-end can be performed by any CMOS foundry whereas the final release step of the mechanical structure is manufactured outside.

III.2.4 – M/NEMS position in the stack and overview

Place taken by M/NEMS devices compared to CMOS circuit and its consequences on the process will be discussed now. The back-end taken for all the following sections will correspond to a standard CMOS foundry one, *i.e.* using Al or Cu as interconnect metallization.

III.2.4.1: M/NEMS below IC

In this approach, the sensing part is processed below the CMOS transistors. One example from the literature is illustrated in Figure I.3.18 and comes from the Delft University of Technology [Raj12]. Rajaraman implemented a co-integrated MEMS-CMOS system using a post-CMOS process. The sensing device was obtained with a grinding and polishing operation of the silicon bulk from an SOI substrate. This substrate thinning required an adhesive bonding of the SOI wafer onto a glass carrier and a final 50µm Si bulk thickness was achieved. Then an ion implantation and a metal deposition (aluminum-silicon alloy, or AlSi here) are fabricated before MEMS patterning device by lithography and DRIE etching. Finally the mechanical structure is released by etching the SOI BOX in hydrofluoric acid (HF) based etchant. The electrical connection is provided by poly-Si interconnects to respect the CMOS compatibility. All these steps were performed at low temperature (≤300°C) according to the post-CMOS approach requirements.

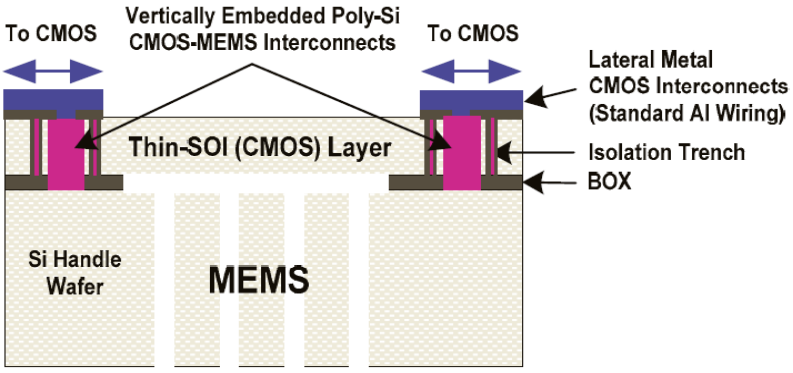


Figure I.3.18: Schematic of a MEMS below-IC device [Raj12].

III.2.4.2: M/NEMS in IC and in Front-End

In such an approach, the M/NEMS device is fabricated in the same level as CMOS circuits. It implies the use of pre or intra-CMOS integration, which allow the possible use of high temperature processes. However the release process corresponds to the most difficult part. Indeed, both the transistors and the metallic interconnections must be protected during this last step. Two examples are illustrated on Figure I.3.19 and I.3.20 developed by the CEA-LETI M/NEMS laboratory. The difference between these developments concerns the manufacture of the transistors: in [Arc12] the CMOS part is performed on the c-Si layer of an SOI substrate using a bulk technology. In [Oll12] the transistors are built using a FDSOI technology. Regarding the sensing device, [Arc12] presents a 1µm thick c-Si MEMS using capacitive detection, and [Oll12] presents a 40nm thick c-Si using a piezo-resistive detection through two nanowire gauges. A cross-section of a nanowire is presented in the inset of the micrograph of Figure I.3.20.

For both these examples, ion implantation and dopant activation through thermal annealing are first performed. After that, the NEMS shape is defined through lithography and etching steps followed by an encapsulation of the mechanical structure with oxide for [Arc12] and poly-Si for [Oll12]. The CMOS devices and the interconnections are then manufactured. Finally the mechanical cantilever is released with vapor HF in [Arc12] and CF_4 in [Oll12]. These etchants respectively remove the oxide and the poly-Si encapsulation layers. In [Arc12] an aperture through the back-end and a deposition of HfO_2 as protective layer were performed in order to protect the passivation, the metallic interconnection and the transistors devices during the HF release. As the CF_4 is really selective compared to the oxide, such protection is not necessary.

Another illustration using this approach comes from the team of Prof. N Barniol from the Autonomous University of Barcelona (UAB) [Vil06]. The process flow is depicted in Figure I.3.21 with a SEM micrograph of the co-integrated system. The heterogeneous system is implemented according to a post-CMOS approach on an SOI wafer (b). After completing CMOS process using a 2.5µm technology (CNM25, from the National Central of Microelectronics [CNM]), capacitive cantilevers are defined by lithography, silicon dry etching and are finally released through wet etching.

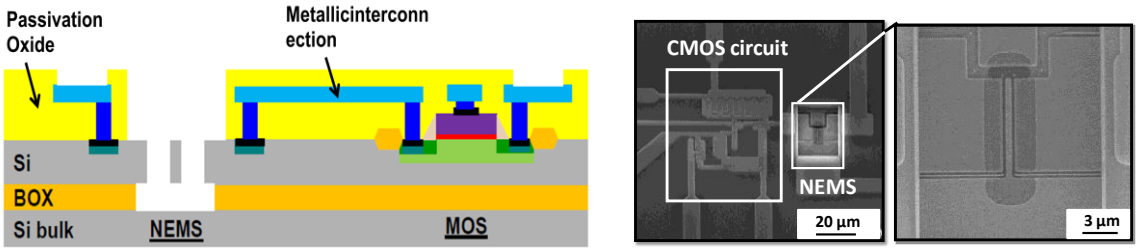


Figure I.3.19: Cross-sectional schematic (left) and SEM micrograph (right) of the front-end NEMS co-integrated with a 0.35µm ST bulk CMOS circuit [Arc12].

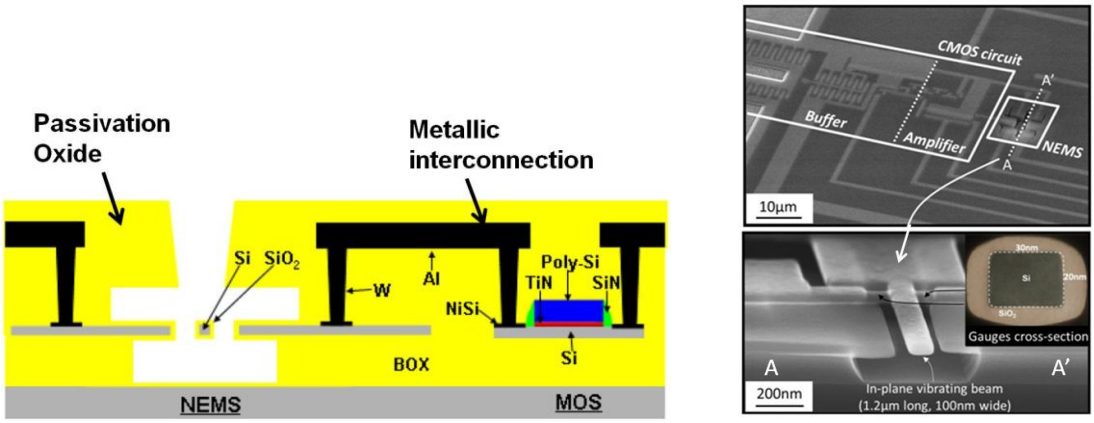


Figure I.3.20: Cross-sectional schematic (left) and SEM micrograph (right) of the front-end NEMS co-integrated with a FDSOI LETI CMOS circuit [Oll12].

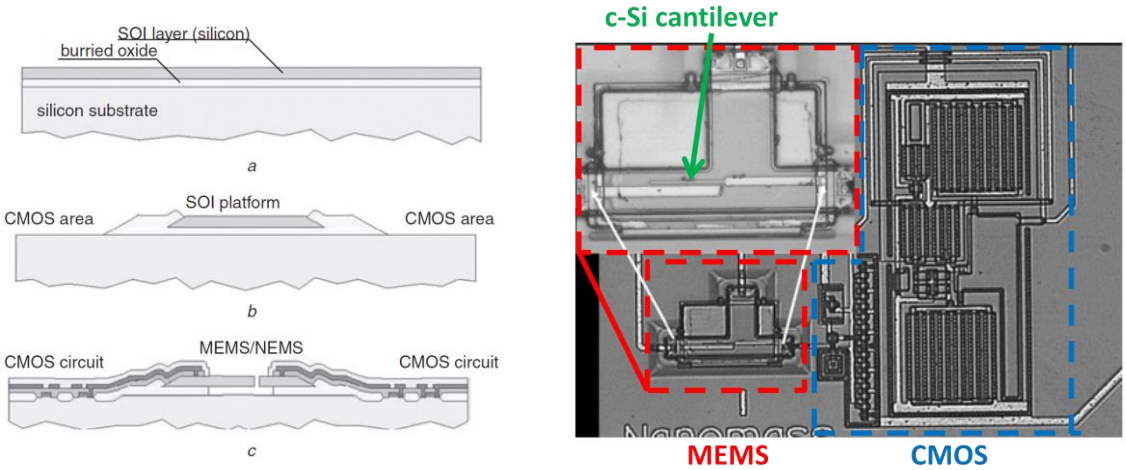


Figure I.3.21: Cross-sectional schematic of the process flow (left) and SEM micrograph of the NEMS-CMOS system (right) [Vil06]. The development was performed on an SOI wafer according to a post-CMOS strategy.

III.2.4.3: M/NEMS in IC and in Middle-End

In this approach, electromechanical devices are manufactured between front-end and back-end zones. The structural layer of resonator can be the poly-Si one which is generally used as capacitors. Intra and post-CMOS can be chosen for such M/NEMS in middle-end strategy, which implies a maximum temperature allowed of 900°C and 500°C respectively for intra and post-CMOS integration. The release process is also critical in order not to damage both the transistors and the back-end. The figures below depict two post-CMOS approaches from state-of-the-art. In Figures I.3.22 and I.3.23 are presented respectively poly-Si dome resonators co-integrated respectively with a 1.5µm ON semiconductor CMOS technology post-processed by the Cornell University – Naval Research Laboratory [Zal10] and a AMS 0.35µm CMOS technology post-processed by N. Barniol's group at UAB [Ver13]. In both implementations, electromechanical devices are defined along the foundry process. The release process constitutes the only step performed outside the foundry. Nevertheless it requires an aperture through the back end in order to have access to the MEMS. A sidewall protection of this aperture can be implemented before the structure release.

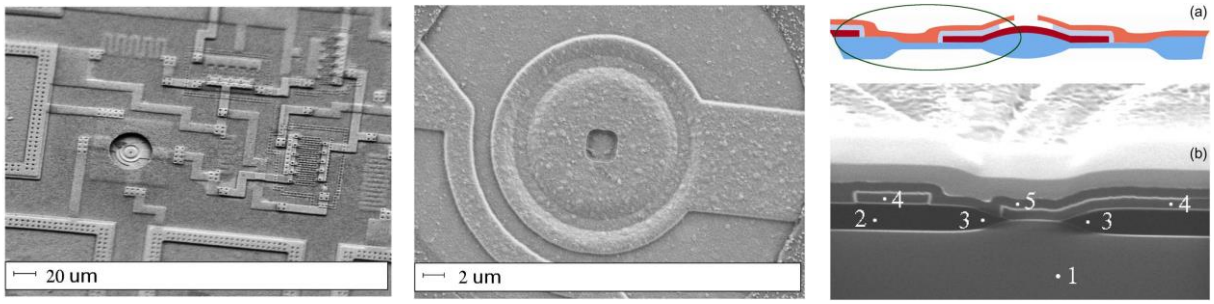


Figure I.3.22: SEM micrograph of the entire MEMS-CMOS system (left) with a zoom on the resonant dome (middle) and its schematic (a) and SEM (b) cross-sectional view (right) [Zal10]. The SEM image on the right indicated the layer used for the mechanical structure. (1) corresponds to Si substrate, (2) and (3) to oxides, (4) to the first poly-Si layer (poly1) and (5) to the second layer of poly-Si (poly2).

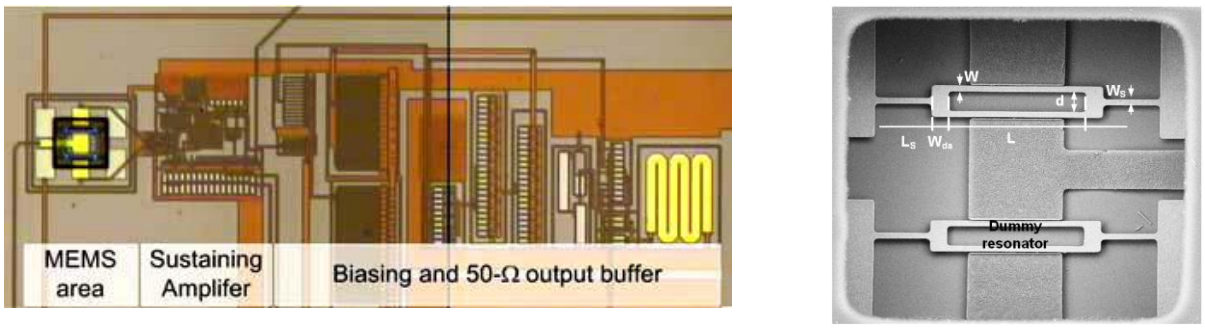


Figure I.3.23: Optical image of the entire co-integrated system (left) with a SEM zoom on the sensing part (right) [Ver13]. The electronic system contains a sustaining amplifier and a buffer. The general electronic circuit for NEMS-CMOS co-integration will be detailed inChapter II.

III.2.4.4: M/NEMS in IC and in Back-End

In this case, back-end materials are used for the MEMS fabrication according to a post-CMOS approach. In this case, sensing device consists of one or several metal layers corresponding to the different interconnection levels. The consequence of such an approach is the thermal budget limited to 400 – 500°C to preserve the integrity of the back-end. Two examples are illustrated in Figures I.3.24 and I.3.25.

Figure I.3.24 (a) (b) and (c) show a capacitive NEMS resonator processed in the fifth level of interconnection metal of a UMC 0.18µm CMOS wafer [Lop09] from UAB. Both cantilevers and local back-end apertures are created along the CMOS process. The only step outside the foundry is the NEMS release by vapor HF etching [Ver06]. This example shows the use of one single metal level.

On Figure I.3.25 is illustrated a MEMS structure using all the back-end metal levels of a TSMC 0.18µm 1P6M CMOS technology [Li13] from the Institute of Nano-engineering and microsystems from the National Tsing Hua University (NTHU) in Taiwan. Like the previous case, the MEMS resonator is manufactured along the CMOS process and the sensing device is released outside the foundry. In this case, no aperture through the back-end is required; a selective etching of the oxide in respect to the metal is enough to release the mechanical structure [Li12]. This approach is also well developed by the group of Prof. W. Fang from NTHU in Taiwan which implemented a lot of sensors following this post-CMOS strategy, such as accelerometer, magnetic, pressure, tactile, temperature sensors etc [Fan13].

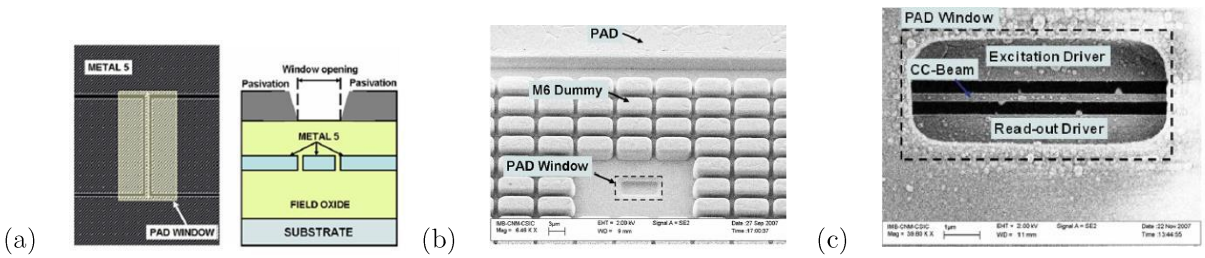
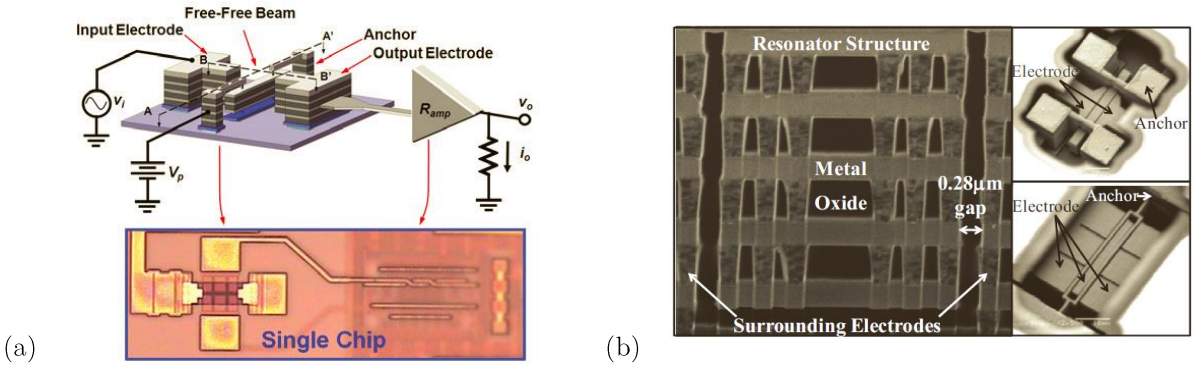


Figure I.3.24: Presentation of the post-CMOS NEMS resonator created in the fifth metal level of a UMC 0.18µm CMOS technology with a presentation of the NEMS layout and a schematic cross-sectional (a), and SEM top views of the stack before release (b) and of the NEMS device (c) [Lop09].

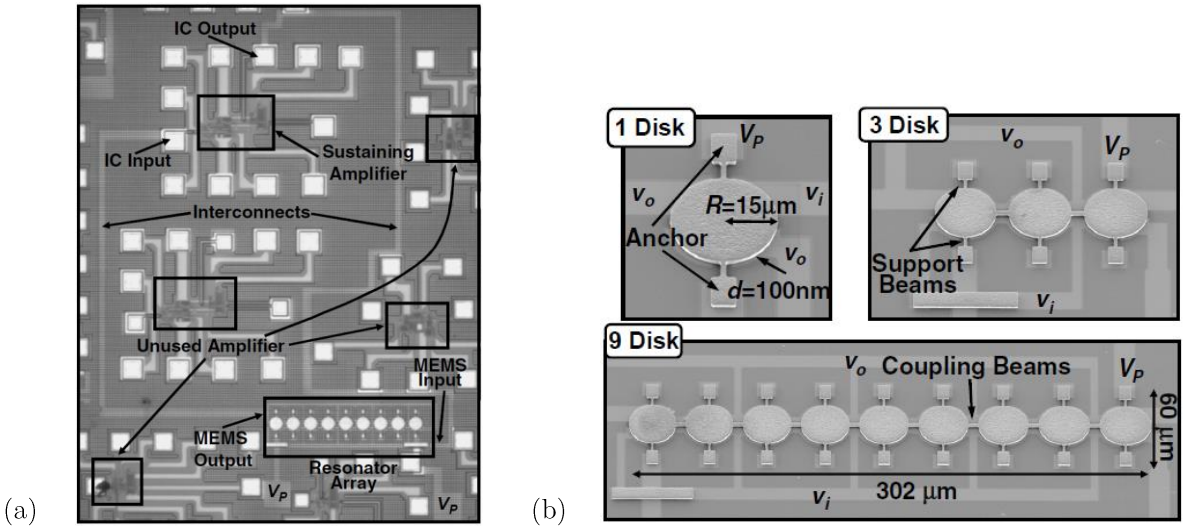


(a) (b)

Figure I.3.25: Presentation of the post-CMOS MEMS-CMOS device using the entire back-end stack as MEMS structural layers. In (a) are depicted a schematic and an optical image of this system. A cross-sectional SEM micrograph and SEM top view of different resonant structures are presented in (b).

III.2.4.5: M/NEMS above-IC

This post-CMOS strategy consists in making the sensing part after and above the back-end. In this situation, mechanic structural layers are deposited at a temperature inferior to the thermal budget limit of the back-end. Because of the presence of the M/NEMS device directly on the surface, this strategy does not require any back-end aperture step before mechanical release operation. The major constraints of this approach are the use of low deposition temperature material for structural layer and for interconnection between NEMS and back-end.



(a) (b)

Figure I.3.26: SEM micrograph of the above-IC CMOS-MEMS device (a) with a focus on the electromechanical resonators (b) [Hua08].

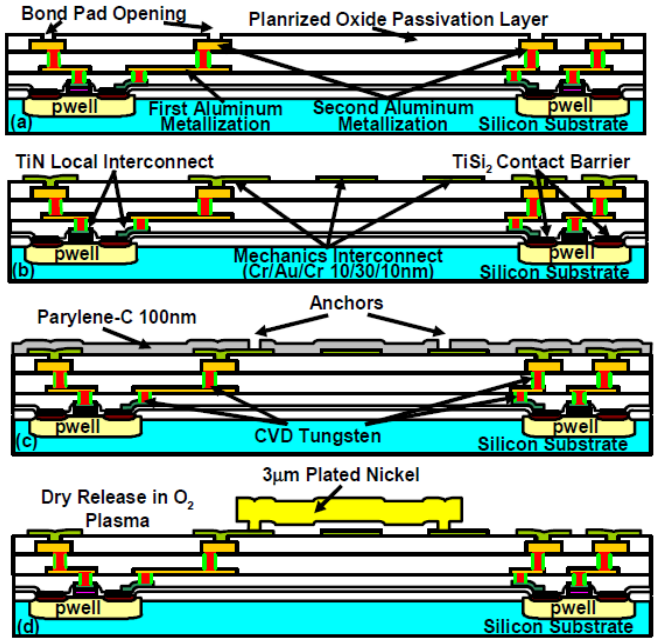


Figure I.3.27: Cross sectional schematic of the above-IC MEMS-CMOS device process flow [Hua08]; (a) CMOS wafer after foundry processing; (b) deposition and patterning of a Cr/Au/Cr trilayer for the electrical interconnection between MEMS and CMOS; (c) CVD deposition of a parylene-C as sacrificial layer followed by a patterning for the anchors definition; (d) electroplating deposition and patterning of Nickel (Ni) as structural material and release of the resonator with isotropic O_2 plasma etching.

The first example (Figures I.3.26 and I.3.27) presented here was performed by the group of Prof. C. T.-C Nguyen (now in Berkeley) at the university of Michigan [Hua08]. The MEMS resonator is fabricated on a 0.35µm 2P4M TSMC CMOS wafer and uses a metal as structural material (nickel here). The maximum temperature used in this example is 50°C including the chromium/gold/chromium (Cr/Au/Cr) trilayer interconnection formation, parylene-C sacrificial layer deposition and electroplating of nickel (Ni) as resonator structural layer. The MEMS release is performed using an isotropic O_2 plasma etching process.

The second example following this approach was performed by IMEC and is presented in Figure I.3.28 [Gon12]. In this paper, the concept of polycrystalline silicon-germanium (poly-SiGe) MEMS co-integrated with 0.13µm CMOS technology circuit was investigated. The CMOS back-end includes two Cu metal interconnection layers (see Figure I.3.28 (a)). The fabrication performed outside the foundry begins with the back-end creation including passivation and electrical connections between the MEMS device and the circuit. Materials used in this step are W and aluminum-copper (AlCu) respectively for vias and metal layers and PECVD silicon oxide for passivation. A planarization by Chemical-Mechanical Polishing (CMP) constitutes the final step before boron-doped SiGe electrodes, MEMS anchors and membranes elaboration. A 3µm thick oxide and poly-SiGe based structures make up the anchors whereas a 3.2µm poly-SiGe deposited by CVD and PECVD techniques patterned structure constitutes the moving membrane.

After that, piezo-resistors are manufactured in poly-SiGe doped by boron implantation. Some etching channels in the membrane are then performed for the subsequent vapor HF removal of the 3µm sacrificial oxide. After the release step, the membrane is sealed with SACVD silicon oxide followed by the creation of piezo-resistor contacts in AlCu. More details of the process are provided on [Gon12]. The maximum temperature achieved in this process is 455°C during 8.5h, corresponding to poly-SiGe deposition and other annealing steps including dopant activation.

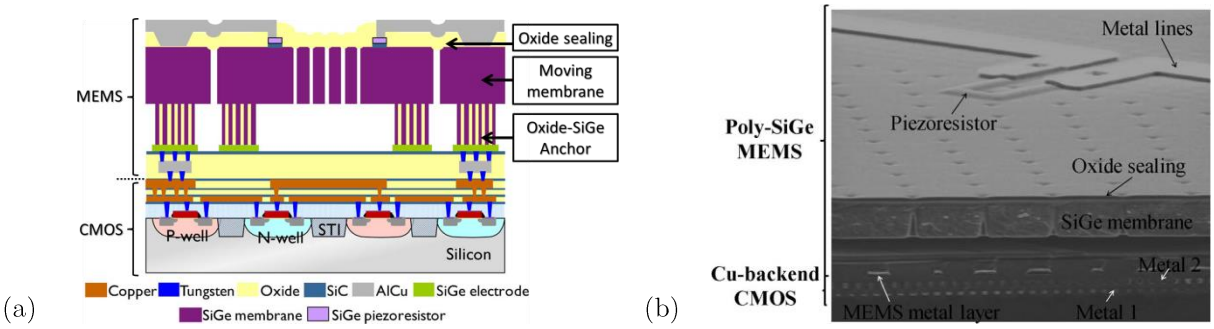


Figure I.3.28: Cross-sectional schematic of the MEMS-CMOS pressure sensor (a) and SEM micrograph cross-section of the MEMS device co-integrated with CMOS back-end (b) [Gon12].

IV. Discussion and conclusion

Different MEMS-CMOS integration strategies were discussed in this chapter with a non-exhaustive overview of several hybrid and monolithic approach implementations. Their different characteristics (see Table I.2) have an influence on sensor fabrication and performance, and have to be confronted with NEMS fabrication specifications:

- Sensing elements must be exposed easily to the outside environment, which is necessary for a better interaction with particles;
- A high sensitivity level and a low resolution level for electromechanical devices are required;
- A short electrical contact and low parasitic capacitances for a better signal transfer between electromechanical devices and electronic circuit is crucial;
- A high density of cantilevers must be provided in order to maximize devices number at the surface and thereby the capture cross-section;
- A low area consumption has to be performed;
- A low cost and simple fabrication (*i.e.* few steps and few requirements) is necessary.

Major advantages and drawbacks are summarized in Table I.3. Hybrid integration simplifies greatly sensor fabrication as every element can be fabricated without impacting on the fabrication of the other one. This approach is furthermore commonly used in industry for SiP (such as assembly using wire bonding, TSVs etc…) and so is reproducible and well-mastered. Even with more technical constraints during fabrication of M/NEMS-CMOS object, monolithic integration appears however as the best option in order to decrease the attenuation during the signal transmission between sensing part and electronic circuit compared to the hybrid integration. This attenuation may be described by the cut-off frequency of the system. The less this frequency is, the more attenuation is. This characteristic will be investigated in the next chapter.

Moreover, as discussed in II.3, p-doped c-Si seems an optimum material for such application thanks to its electromechanical properties, for example Young modulus, stiffness, high elastic range and so on. Two monolithic integrations seem to satisfy this criterion: NEMS in FE and NEMS above-IC. These strategies will be more explored in the two subsequent chapters.

Technology	Hybrid Integration							Monolithic integration		
	Wire bonding	TLP	µ-bump	µ-insert	µ-tube	Direct metal-oxide bonding	TSV	Below-IC	In-IC	Above-IC
# masks[a]	0	5	3	3	5	1 (for metal bonding)	2[b]	~2 (for int. fabrication)	1 (for MEMS aperture)	~2 (for int. fabrication)
Fabrication steps[a]	1	<15	<15	<15	<20	<10	>20	<5	<5	<5
Assembly temperature	Ambient	<300° C	<250°C	150°C	Ambient	400°C	400°C	<900°C (intra) <450°C (post CMOS)	<900°C (FE) <450°C (BE)	<450°C
T-C[c] required?	No	Yes	No	Yes	Yes	No	No	No	No	No
P[d]. requirements	--	<1µm	<4µm	<3µm	<1.5µm	<0.5nm	[b]--	No	No	No
Integration	D2D, D2W	D2D, D2W	D2D, D2W	D2D, D2W	D2D, D2W	D2D, D2W, W2W	D2D, D2W, W2W	W2W	W2W	W2W
Int.diameter Int. length	~50µm ~0.1 to 10cm	~5µm ~10µm	~10µm ~10µm	~5µm ~5µm	~5µm ~5µm	~5µm ~5µm	2-10µm 15-100µm	Depending on the CMOS technology		
Int.pitch	~50µm (PAD pitch)	~10µm	15 to 50µm	<20µm	~10µm	<10µm	10-20µm			
Int. material	Au, Al	Au-In, Cu-Sn	In, Cu-SnAgCu	Au, Ni	WSi, Au	SiO_2, Cu, TiN	TiN, Cu (Via-Middle and Via-Last)	W, poly-Si	AlCu, AlSi, Cu	AlCu, AlSi, Cu
							W, poly-Si (Via-First)			
Pitch restricted by	Metal pads	Int.	Int.	Int.	Int.	NEMS	Int.	NEMS		
Int. resistance Int. capacitance	~1-100mΩ ~10pF	~10mΩ --	~10mΩ --	~100mΩ --	~100mΩ --	~10mΩ --	~100mΩ ~100fF	~10mΩ ~10fF	~10mΩ ~10fF	~10mΩ ~10fF

[a] : does not take into account the M/NEMS and the CMOS realizations; [b]: only for TSV formation (assembly technique not taken into account); [c]: for thermo-compression; [d]: for planarity; Int. stands for interconnection.

Table I.2: Main characteristics for each assembly technology.

Technology	Hybrid integration				Monolithic integration		
	Wire bonding	3D Interconnects	Direct metal-oxide bonding	TSV	Below-IC	In-IC	Above-IC
Advantages	-Very simple method - No impact on CMOS and MEMS technology - Low electrical resistance	- Pre-test possible before final assembly - High yield - High flexibility with respect to the CMOS technology - Low electrical resistance - No parasitic capacitances	- Few fabrication steps - Low interconnection pitch - Thermo-compression not required - W2W integration possible - Low electrical resistance - No parasitic capacitances	-Thermo-compression not required - W2W integration possible - No encapsulation of the sensing part - Low electrical resistance	- Sensing part directly in contact with environment - Possible use of c-Si as structural material for MEMS - Low parasitic capacitances	- MEMS fabricated along the CMOS process (in ME and BE configuration) - Cu/Al possible as interconnection material - c-Si as structural material for MEMS (in FE configuration) - Low parasitic capacitances	- High flexibility with respect to the CMOS technology - No encapsulation of the sensing part - Low area consumption - Low parasitic capacitances
Drawbacks	- Large area consumption - Large parasitic capacitances leading to strong signal attenuation	- Many fabrication steps - W2W integration not possible - Low production throughput - Encapsulation of the sensing part - Thermo-compression required - High interconnection pitch	- High planarity and alignment requirements - Encapsulation of the sensing part	- High interconnection pitch - High interconnection resistance - Large parasitic capacitances leading to signal attenuation	- Interconnection compatible with FE (Cu/Al use forbidden) - Necessary modification of the CMOS process - Many fabrication steps	- Modification of CMOS process necessary (in FE approach) - c-Si MEMS not possible (in ME and BE approach) - No use of high temperature processes - Encapsulation of the sensing part - Large area consumption	- No use of high temperature processes - c-Si based MEMS not possible -Necessary protection of the CMOS

Table I.3: Summary of main advantages and drawbacks for each approach.

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Chapter II

An experimental demonstration of 2D NEMS-CMOS monolithic co-integration

In the first chapter was presented a brief overview of different integration schemes to fabricate sensors associating NEMS resonators and a CMOS readout circuit. The monolithic approach appears as the best way to implement such a device compared to the different hybrid options. This chapter focuses on the electrical performance of monolithic NEMS-CMOS systems. It first deals with a brief analysis of signal transmission properties for each assembly technique. In a second time, a modelling study of a nano-resonator is proposed and confronted with electrical characterizations. From these experimental results, devices parameters are extracted and exploited to demonstrate the operation of a NEMS-CMOS self-oscillator.

I. Signal transmission properties of different interconnection ways

I.1 Introduction

Different integration schemes were previously analyzed taking into account the process fabrication and the dimensional characteristics of interconnects. The signal transmission between sensing and electronic part is also a crucial parameter since a strong attenuation leads to a low signal-to-noise ratio (SNR[10]). The useful NEMS signal may be thereby lost in the noise, affecting the sensor resolution. This first section proposes a brief study of signal attenuation for each assembly technique. This analysis is performed using a small ac-signal modelling with a frequency between 1MHz – 1GHz and focuses on the frequency response of the device, more particularly on the gain. The selected frequency range corresponds to the one usually used for NEMS-based mass detection.

I.2 Interconnects attenuation

I.2.1 – System presentation

To evaluate the attenuation properties of each interconnect, a system comprising three different parts is considered: a NEMS resonator is linked to an interconnect and a CMOS circuit (Figure II.1.1). A source with an impedance Z_E is connected to the electromechanical system. R_{NEMS} corresponds to the electrical resistor between the NEMS device and the interconnections including the doped silicon series resistance of the corresponding routing, and the contact resistance between the metal and the nano-resonator. A value of 1kΩ is taken for this resistance. Figure II.1.2 depicts the electrical model used for the CMOS circuit. The latter is represented as a resistance R_{elec} corresponding to the total electrical resistance between the interconnections and the transistor (*i.e.* metal layers, vias and contact resistances) associated with a capacitance C_{elec} symbolizing the gate-source capacitance of the transistor. $V_{in\text{-}elec}$ and V_{elec} are respectively the input voltage and the gate voltage.

[10] This notion will be more explained in section II.

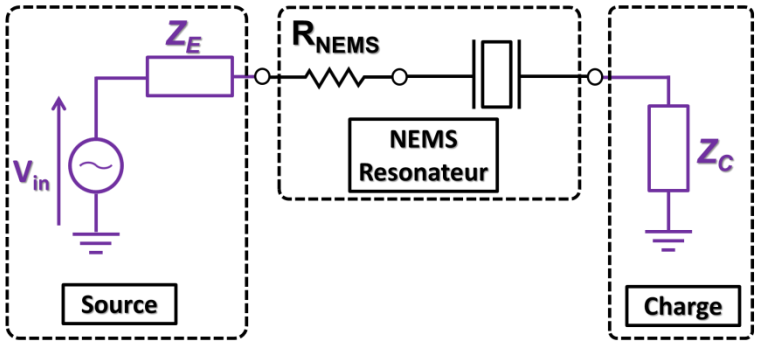
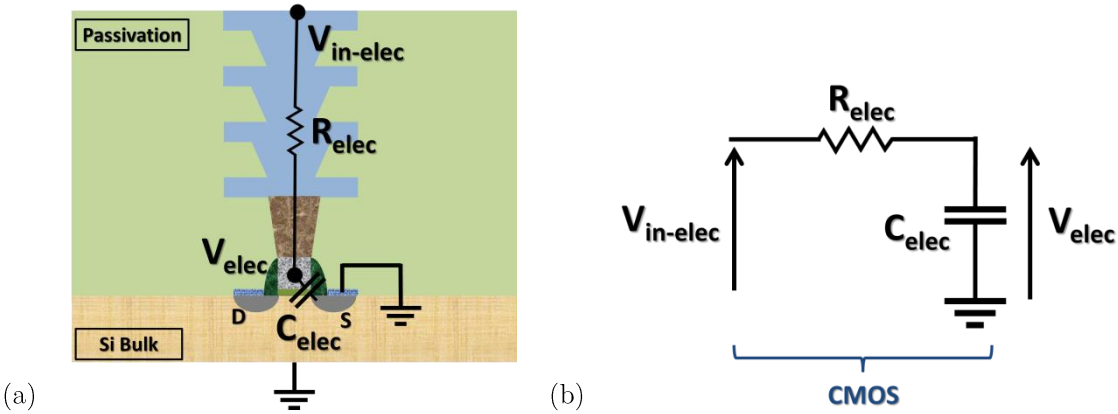


Figure II.1.1: Electrical schematic of the system. The load impedance Z_C consists of the interconnect and the electronic circuit. The input of the NEMS resonator is linked to a source with an output impedance Z_E generating the voltage V_{in}.



(a) (b)

Figure II.1.2: (a) Cross-sectional schematic of the CMOS circuit symbolized by a transistor and its interconnections with its small signal electrical model (b). S and D respectively stand for the transistor source and drain.

For this study, all the system is placed at the NEMS resonance. Consequently, the resonator can be modelled as an impedance Z_M so-called the motional impedance which corresponds to the NEMS impedance at its resonance frequency[11].Considering the values of the motional impedance (reported in Table II.1), the source impedance (typically 50Ω) and the resistance R_{NEMS}, both Z_E and R_{NEMS} can be neglected with respect to Z_M. The system {NEMS - source} can be modelled as a source with an impedance Z_M as represented in Figure II.1.3. With this representation, V_{in} becomes V_{NEMS} and corresponds to the signal generated by the nano-resonator.

[11]These notions will be more explained in section II.

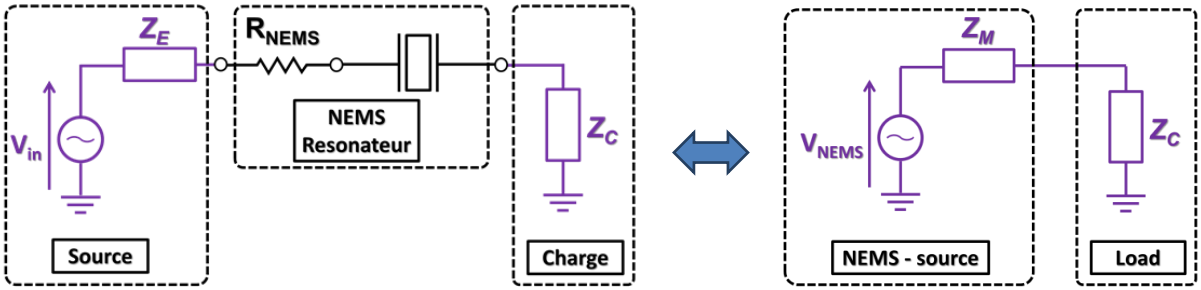


Figure II.1.3: Simplification of the system {NEMS - source} for the signal attenuation study.

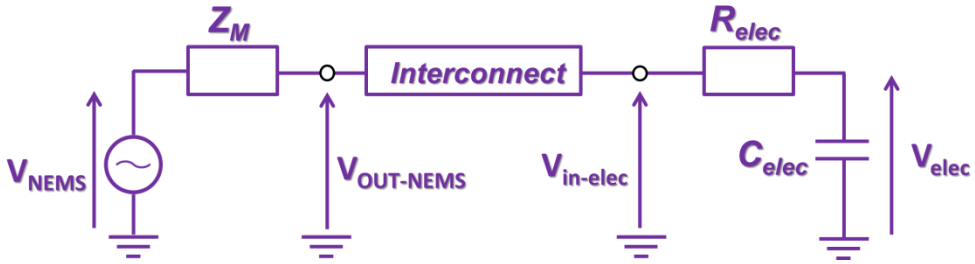


Figure II.1.4: Schematic representation of a generic system {NEMS-interconnect-CMOS circuit} used as case study.

Figure II.1.4 depicts the system used for the signal attenuation study of different types of interconnects. All of them are represented by their transfer function $H_{interco}$ defined in (II.1). $V_{OUT\text{-}NEMS}$ corresponds here to and the input voltage of the interconnect.

$$H_{interco} = \frac{V_{elec}}{V_{NEMS}} \tag{II.1}$$

The goal is to calculate $H_{interco}$ for each type of interconnection and to determine its frequency response. Values of the electrical parameters for the NEMS impedance and the CMOS circuit are given in Table II.1.

Electrical element	Z_M	R_{elec}	C_{elec}
Value	1MΩ	10Ω	1pF

Table II.1: Parameters selected for the study of the interconnection signal attenuation.

I.2.2 – TSVs

Figure II.1.5 (a) and (b) show the electrical model taken to determine the signal attenuation of TSVs. This model is used in many papers [Cad10-Ryu06-Kim14]. Table II.2 summarizes the values for each element of the TSV according to [Cad10]. Here the frequency response of a TSV with a 4µm diameter (ϕ_{TSV}) and a 15µm depth (h_{SV}) is investigated. R_{TSV}, L_{TSV}, C_{TSV}, C_{Si}, G_{Si} and C_P respectively characterize the resistance, inductance and capacitance of the TSV, the capacitance and the conductance of the silicon bulk and the parasitic capacitance between the electromechanical device and the pad. According to Figure II.1.5 (b), the transfer function H_{TSV} can be determined:

$$H_{TSV} = \frac{V_{elec}}{V_{NEMS}} = \frac{V_{elec}}{V_{in-elec}} \cdot \frac{V_{in-elec}}{V_A} \cdot \frac{V_A}{V_{NEMS}} = H_{elec} \cdot H_{TSV-2} \cdot H_{TSV-1} \tag{II.2}$$

H_{TSV} is decomposed into three parts for simplification defined as:

$$H_{TSV-1} = \frac{V_A}{V_{NEMS}} \qquad H_{TSV-2} = \frac{V_{in-elec}}{V_A} \qquad \text{and} \qquad H_{elec} = \frac{V_{elec}}{V_{in-elec}} \tag{II.3}$$

The development of these three transfer functions gives:

$$H_{elec}(\omega) = \frac{1}{1 + jR_{elec}C_{elec}\omega} = \frac{1}{1 + j\,f/f_{elec}} \tag{II.4}$$

$$H_{TSV-2}(\omega) = \frac{1 + j\frac{C_{Si}}{G_{Si}}\omega + j\frac{C_{TSV}}{G_{Si}}\omega}{1 + j\frac{C_{Si}}{G_{Si}}\omega + j\frac{C_{TSV}}{G_{Si}}\omega + jR_{TSV}C_{TSV}\omega - L_{TSV}C_{TSV}\omega^2 - \frac{C_{Si}R_{TSV}C_{TSV}}{G_{Si}}\omega^2 - j\frac{C_{Si}L_{TSV}C_{TSV}}{G_{Si}}\omega^3} \tag{II.5}$$

$$H_{TSV-2}(f) = \frac{1 + j\,f/f_{Si} + j\,f/f_{Si-TSV}}{1 + j\,f/f_{Si} + j\,f/f_{Si-TSV} + j\,f/f_{TSV} - f^2/f_{0-TSV}^2 - f^2/f_{Si} \cdot f_{TSV} - j\,f^3/f_{Si} \cdot f_{0-TSV}^2} \tag{II.6}$$

$$H_{TSV-1}(\omega) = \frac{1 + jR_{Si}C_{Si}\omega + jR_{Si}C_{TSV}\omega}{1 + jZ_MC_{TSV}\omega \cdot (1 + jR_{Si}C_{Si}\omega) + jZ_MC_P\omega + jR_{Si}C_{Si}\omega + jR_{Si}C_{TSV}\omega - R_{Si}C_{Si}Z_MC_P\omega^2 - R_{Si}C_{TSV}Z_MC_P\omega^2} \tag{II.7}$$

$$H_{TSV-1}(f) = \frac{1 + j\,f/f_{Si} + j\,f/f_{Si-TSV}}{1 + j\,f/f_{Si} + j\,f/f_{Si-TSV} + j\,f/f_{NEMS-p} + j\,f/f_{NEMS-TSV} \cdot \left(1 + j\,f/f_{Si}\right) - f^2/f_{Si} \cdot f_{NEMS-p} - f^2/f_{Si-TSV} \cdot f_{NEMS-p}} \tag{II.8}$$

F and ω respectively represent the frequency (in Hz) and the pulsation (in rad.s^{-1})[12]. All the frequency noted $f_{Si,}$; $f_{Si\text{-}TSV}$; $f_{NEMS\text{-}TSV}$; $f_{NEMS\text{-}p}$; $f_{TSV;}$ and $f_{0\text{-}TSV}$ are introduced and defined in Table II.3.

Electricalelement	R_{TSV}	C_{TSV}	L_{TSV}	C_{Si}	G_{Si}	C_P
Value	70mΩ	100fF	4pH	10fF	0.5mS	10fF

Table II.2: Parameters selected for the study of the TSV signal attenuation (inspired from [Cad10]).

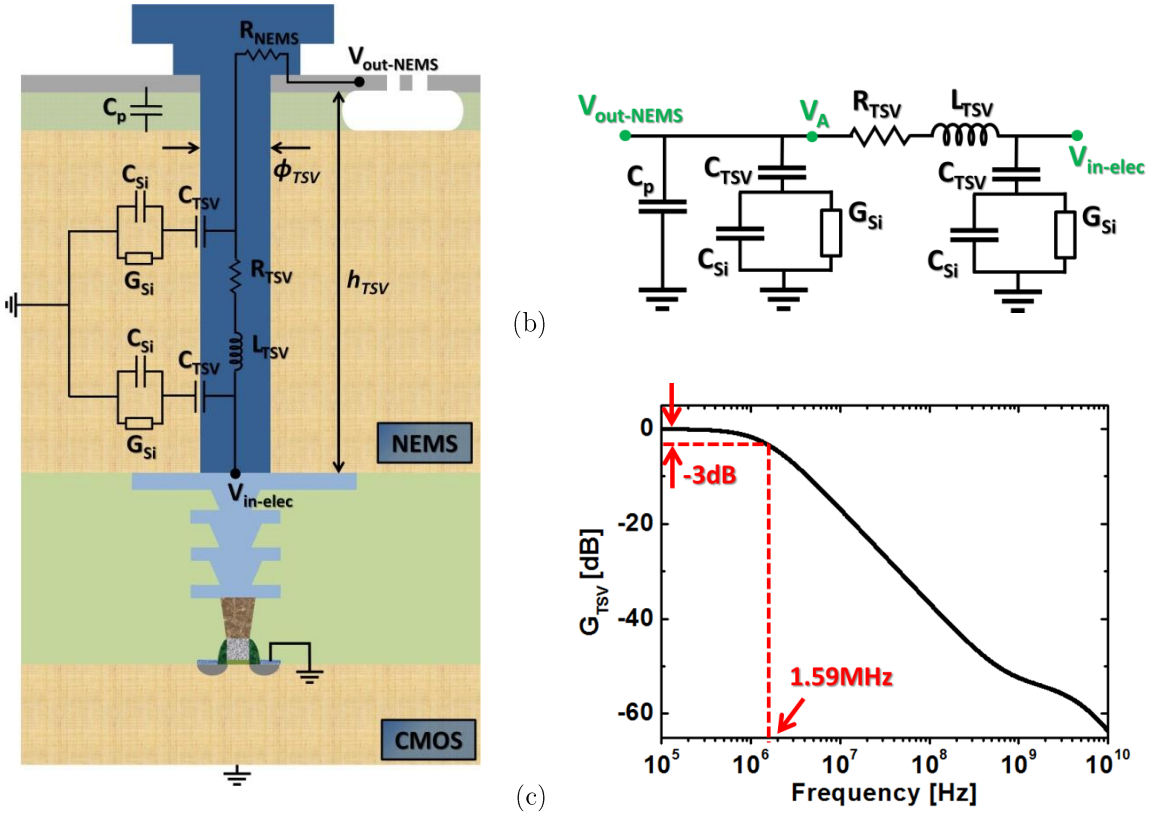


Figure II.1.5: (a) Cross-sectional schematic of a TSV interconnecting a NEMS device to a CMOS circuit with its electrical model (b) (inspired from [Cad10]) and its frequency response (c).

Frequencies	f_{Si}	$f_{Si\text{-}TSV}$	$f_{NEMS\text{-}TSV}$	$f_{NEMS\text{-}p}$	f_{TSV}	$f_{0\text{-}TSV}$
Definition	$\frac{G_{Si}}{2\pi \cdot C_{Si}}$	$\frac{G_{Si}}{2\pi \cdot C_{TSV}}$	$\frac{1}{2\pi \cdot Z_M C_{TSV}}$	$\frac{1}{2\pi \cdot Z_M C_p}$	$\frac{1}{2\pi \cdot R_{TSV} C_{TSV}}$	$\frac{1}{2\pi \cdot \sqrt{L_{TSV} C_{TSV}}}$
Value	7.96GHz	796MHz	1.59MHz	15.9MHz	22.7THz	251GHz

Table II.3: Definition and value of the different frequencies present in (II.6) and (II.8).

Signal attenuation with TSVs can be afterwards calculated through G_{TSV} as:

$$G_{TSV}(\omega) = 20 \cdot \log_{10}\left[\left|H_{TSV}(\omega)\right|\right] \qquad \text{(II.9)}$$

[12] f and ω are linked through this equation: $\omega = 2\pi f$

From Figure II.1.5 (c), the cut-off frequency[13] of the entire system is evaluated around 1.59MHz. Consequently, typical NEMS signals, which are below 2MHz, will not be attenuated before arriving at the CMOS circuit input.

I.2.3 – Wire bonding

Figure II.1.6 (a) and (b) depict the electrical model used for the determination of the signal attenuation of a gold bond wire. The model taken for the substrate is identical to the one presented in the previous section. The parasitic capacitance C_{WB} of a bond wire was chosen according to [Arn11]. Its resistance is evaluated in (II.10). Considering a wire with a length L_{wire} of 1cm and a diameter ϕ_{wire} of 100µm, R_{WB} is evaluated around 30mΩ.

$$R_{WB} = \rho_{Au} \frac{L_{wire}}{\pi\left(\Phi_{wire}/2\right)^2} \quad [\Omega] \tag{II.10}$$

The transfer function H_{WB} is defined as:

$$H_{WB} = \frac{V_{in-elec}}{V_{NEMS}} \cdot \frac{V_{elec}}{V_{in-elec}} = H_{WB\text{-}1} \cdot H_{elec} \tag{II.11}$$

According to Figure II.1.6 (b), $H_{WB\text{-}1}$ is given by:

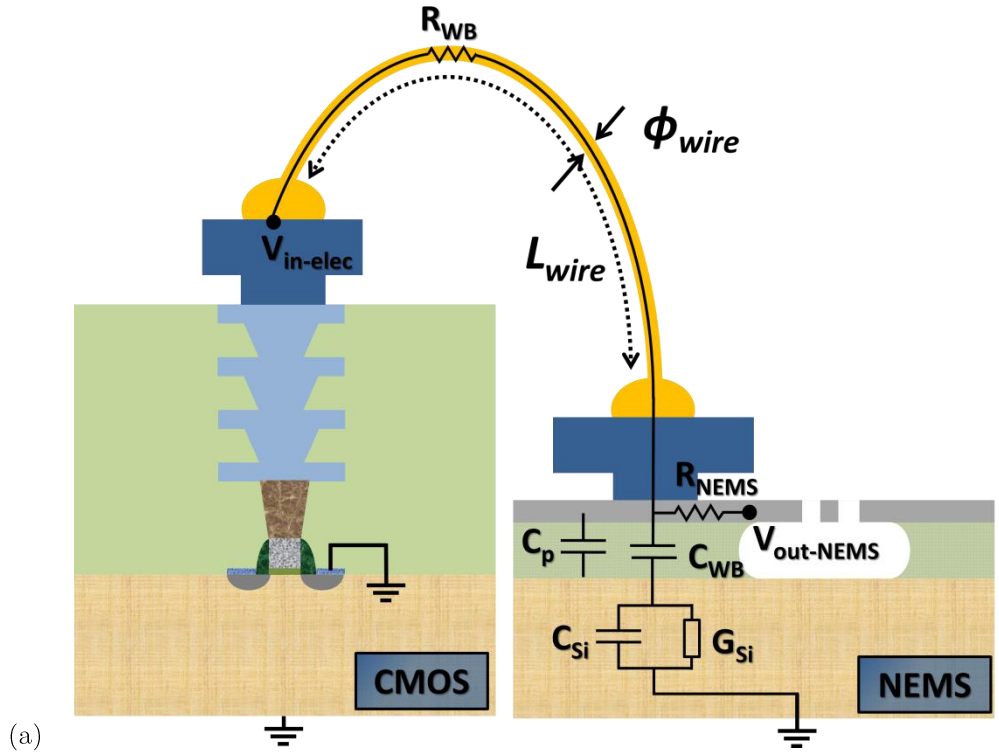
$$H_{WB\text{-}1}(\omega) = \frac{1 + j\frac{C_{Si}}{G_{Si}}\omega + j\frac{C_{WB}}{G_{Si}}\omega}{1 + j\frac{C_{Si}}{G_{Si}}\omega + j\frac{C_{WB}}{G_{Si}}\omega + jZ_M C_P\omega + jZ_M C_{WB}\omega \cdot \left(1 + j\frac{C_{Si}}{G_{Si}}\omega\right) - \frac{C_{WB}Z_M C_P}{G_{Si}}\omega^2 - \frac{C_{Si}Z_M C_P}{G_{Si}}\omega^2} \tag{II.12}$$

$$H_{WB\text{-}1}(f) = \frac{1 + j\,f/f_{Si} + j\,f/f_{Si-WB}}{1 + j\,f/f_{Si} + j\,f/f_{Si-WB} + j\,f/f_{NEMS-p} + j\,f/f_{NEMS-WB} \cdot \left(1 + j\,f/f_{Si}\right) - f^2/f_{Si-WB} \cdot f_{NEMS-p} - f^2/f_{Si} \cdot f_{NEMS-p}} \tag{II.13}$$

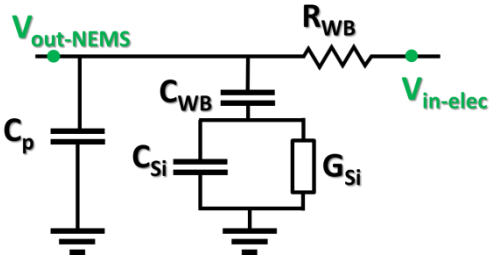
The corresponding gain is:

$$G_{WB}(\omega) = 20 \cdot \log_{10}\left[\left|H_{WB}(\omega)\right|\right] \tag{II.14}$$

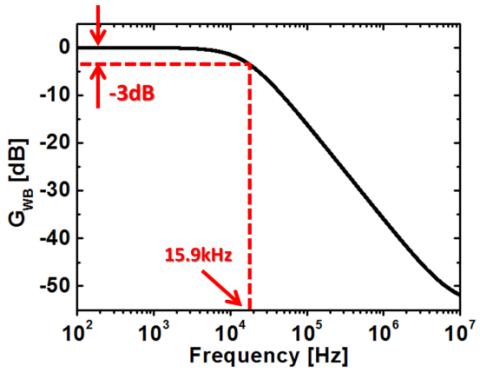
[13]The cut-off frequency f_c of a system corresponds to the frequency in which a 3dB attenuation with respect to the gain at low frequency is measured, *i.e.* $G(f_c)=G(f\sim0)-3dB$. This datum is usually used to characterize the signal transmission property of a system.



(a)



(b)



(c)

Figure II.1.6: (a) Cross-sectional schematic of a wire-bonding interconnection between a NEMS device and a CMOS transistor with its electrical model (b) and its frequency response (c).

Table II.4 and II.5 respectively summarize the values for each element of the bond wire and the different cut-off frequency values.

Electrical element	R_{WB}	C_{WB}	C_{Si}	G_{Si}	C_P
Value	28mΩ	10pF	10fF	0.5mS	10fF

Table II.4: Parameters taken for the study of a bond wire signal transmission.

Cut-off frequencies	f_{Si}	$f_{Si\text{-}WB}$	$f_{NEMS\text{-}WB}$	$f_{NEMS\text{-}p}$
Definition	$\frac{G_{Si}}{2\pi \cdot C_{Si}}$	$\frac{G_{Si}}{2\pi \cdot C_{WB}}$	$\frac{1}{2\pi \cdot Z_M C_{WB}}$	$\frac{1}{2\pi \cdot Z_M C_p}$
Value	7.96GHz	7.96MHz	15.9kHz	15.9MHz

Table II.5: Definition and value of the different frequencies present in (II.13).

In this case, the cut-off frequency is as low as 15kHz (see Figure II.1.6 (c)). Wire-bonding is therefore not recommended for NEMS-CMOS assembly.

I.2.4 – 3D interconnects and metal-oxide direct bonding

This section will focus on the electrical performance of various NEMS-CMOS interconnection schemes such as direct metal-oxide bonding, 3D interconnects like TLP, µ-bump, µ-insert and µ-tube. For the attenuation determination, both bulk and BOX parts of the SOI substrate used for NEMS implementation are removed, as it could be for the sensor fabrication. Such an assembly is illustrated in Figure II.1.7 (a). In all cases, the interconnection parasitic capacitance is determined and indicated in Table II.6. Two values are chosen for this capacitance: 0 for TLP, µ-bump and direct metal-oxide bonding since the opposite surfaces present in these interconnects can be neglected; and C_{int} for µ-insert and µ-tube, represented in Figure II.1.7 (a) and defined in (II.15). ε_0, S_{int} and d_{int} respectively represent the vacuum permittivity (in F.m^{-1}), the area (in m^2) and the gap (in m) of the capacitance. The expression of S_{int} is given in (II.16) where r_{int} (in m) corresponds to the interconnect radius. The values chosen for the interconnect dimensions are given in Table II.7.

$$C_{\text{int}} = \frac{\varepsilon_0 \cdot S_{\text{int}}}{d_{\text{int}}} \ [\text{F}] \qquad \text{(II.15)}$$

$$S_{\text{int}} = \pi \cdot r_{\text{int}}^2 \ [\text{m}^2] \qquad \text{(II.16)}$$

Interconnect nature	TLP	µ-bump	µ-insert	µ-tube	Direct metal-oxide bonding
Capacitance value	0	0	C_{int}	C_{int}	0

Table II.6: Capacitance values chosen according to the interconnect.

Geometricelement	r_{int}	d_{int}
Value	2.5µm	2µm

Table II.7: Geometric values taken for the interconnect capacitance [Col13].

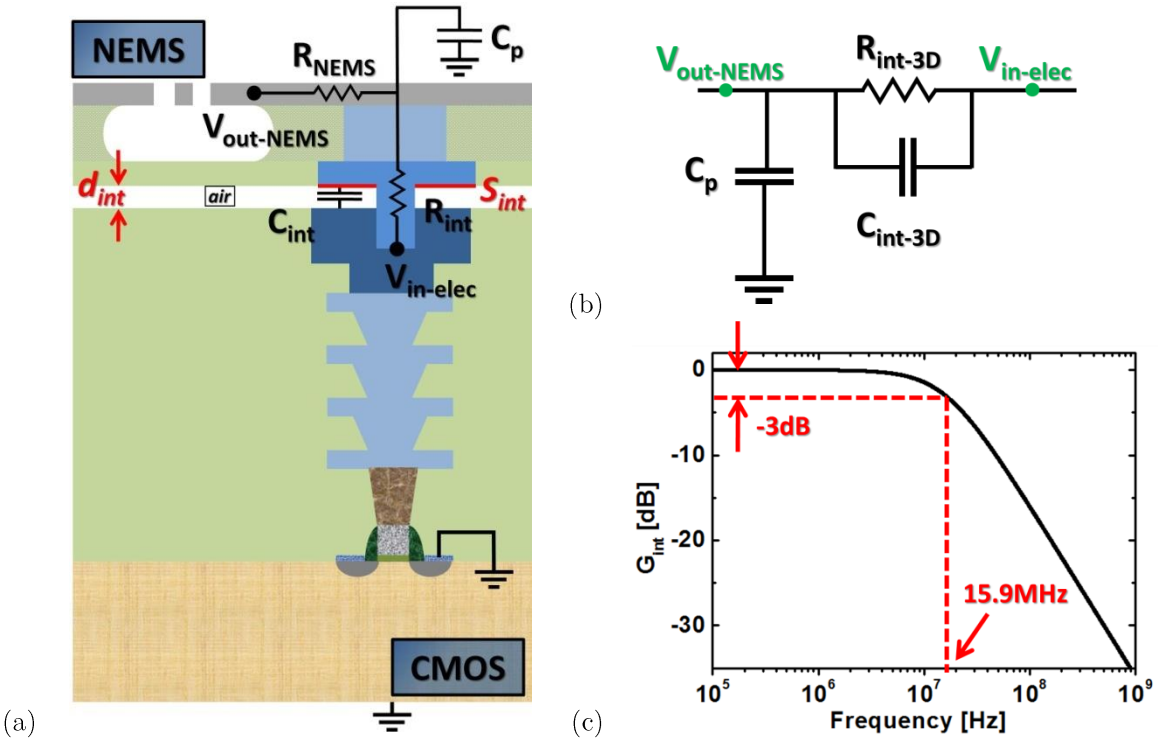


Figure II.1.7: (a) Cross-sectional schematic of 3D interconnect and metal-oxide direct bonding with its electrical model (b) and its frequency response (c).

According to Figure II.1.7 (a) and (b), the interconnect impedance Z_{int} can be expressed as (II.17) where R_{int} and C_{int} respectively correspond to the resistance and the capacitance of the interconnect.

$$Z_{\text{int}}(\omega) = \frac{R_{\text{int}}}{1 + jR_{\text{int}}C_{\text{int}}\omega} \quad [\Omega] \tag{II.17}$$

According to the value of R_{int} and C_{int} presented in Table II.8, the cut-off frequency f_{int} can be calculated (see Table II.9). For a frequency between 1MHz and 1GHz, the term $R_{int}C_{int}\omega$ can be neglected with respect to 1, simplifying the interconnect model which can be considered as a resistance R_{int}. Consequently, the transfer function of the system defined in (II.18) can be expressed according to (II.19):

$$H_{\text{int}} = \frac{V_{elec}}{V_{in-elec}} \cdot \frac{V_{in-elec}}{V_{NEMS}} = H_{elec} \cdot H_{\text{int}-1} \tag{II.18}$$

$$H_{\text{int}-1}(\omega) = \frac{1}{1 + jZ_M C_p \omega} \tag{II.19}$$

The values presented in Table II.8 allow the determination of the cut-off frequency $f_{NEMS\text{-}p}$ (see Table II.9). The gain of the system, expressed in (II.20), is plotted in Figure II.1.7 (c).

$$G_{\text{int}}(\omega) = 20 \cdot \log_{10}\left[\left|H_{\text{int}}(\omega)\right|\right] \tag{II.20}$$

Electricalelement	R_{int}	C_{int}	C_P
Value	100mΩ	100aF	10fF

Table II.8: Parameters of the study of 3D interconnect signal attenuation.

Cut-off frequencies	f_{int}	$f_{NEMS\text{-}p}$
Definition	$\frac{1}{2\pi \cdot R_{\text{int}} C_{\text{int}}}$	$\frac{1}{2\pi \cdot Z_M C_p}$
Value	$1.59\text{x}10^9$ GHz	15.9MHz

Table II.9: Parameters of the study of 3D interconnect attenuation.

In this case, the signal attenuation does not come from the interconnect, but only by the NEMS and the layout parasitic capacitance C_P. Figure II.1.7 (c) shows that the cut-off frequency is as high as 15.9MHz.

I.2.5 – Monolithic integration

The signal attenuation of a monolithic NEMS-CMOS integration scheme is investigated in this section. Figure II.1.8 depicts a cross-sectional schematic and the electrical model for a 2D and 3D co-integration. The transfer function is defined by (II.21) and can be developed in (II.22) according to the model.

$$H_{mono} = \frac{V_{elec}}{V_{in-elec}} \cdot \frac{V_{in-elec}}{V_{NEMS}} = H_{elec} \cdot H_{mono-1} \tag{II.21}$$

$$H_{mono-1}(\omega) = \frac{1}{1 + jZ_M C_p \omega} \tag{II.22}$$

The gain defined in (II.23) can be calculated with the values of R_{NEMS} and C_p taken from the previous tables, and plotted (see Figure II.1.8 (d)).

$$G_{mono}(\omega) = 20 \cdot \log_{10}\left[\left|H_{mono}(\omega)\right|\right] \tag{II.23}$$

As observed in 3D interconnects and in metal-oxide direct bonding cases, only signals beyond 15.9MHz are attenuated.

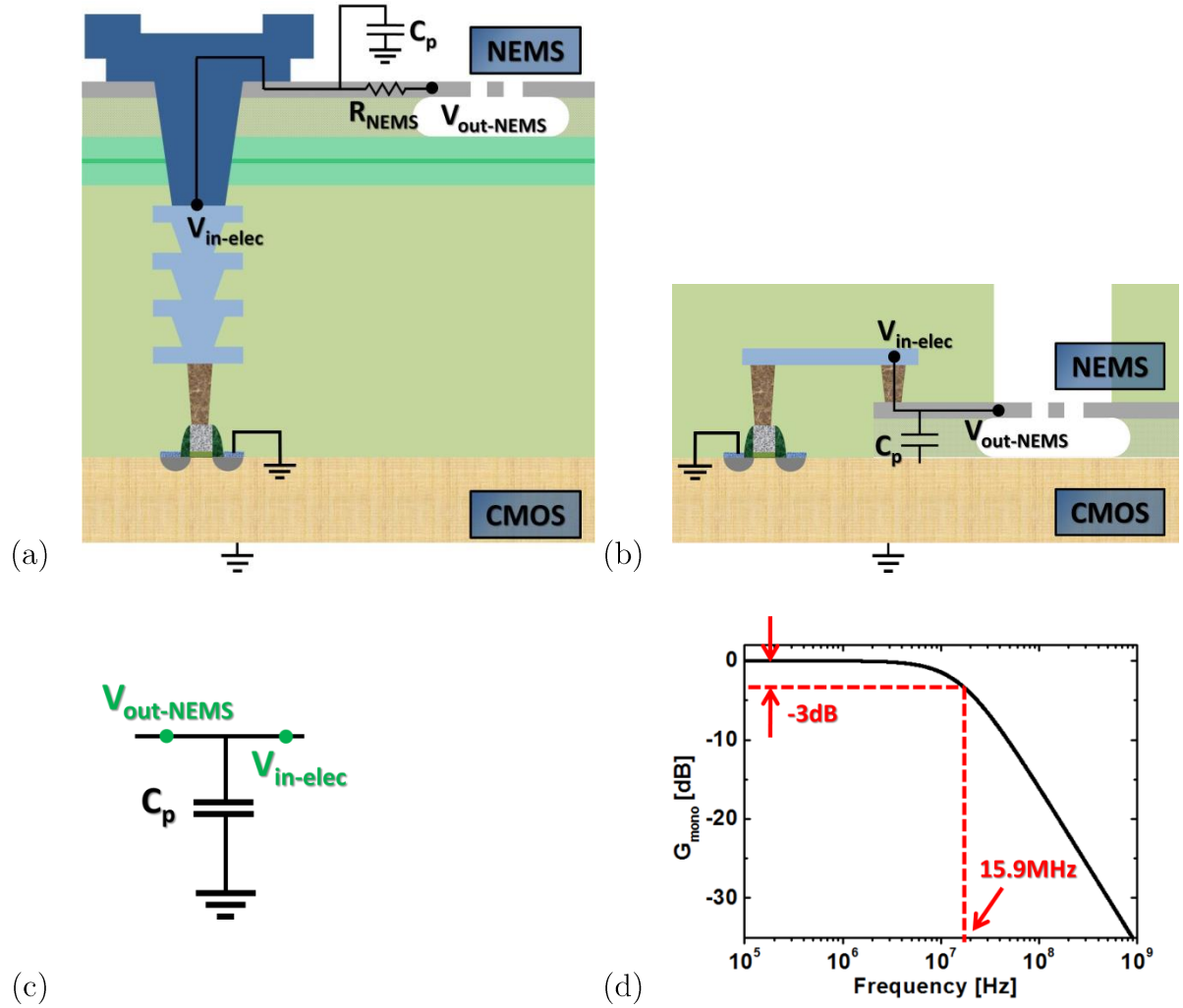


Figure II.1.8: Cross-sectional schematic of a monolithic 3D (a) and 2D (b) co-integration between NEMS and CMOS with its electrical model (c) and its frequency response (d).

I.3 Conclusion

This first part has analyzed signal attenuation for various assembly methods. A summary is provided in Table II.10 which gives the different cut-off frequencies. Monolithic integration shows an outstanding signal transmission between NEMS and CMOS since the cut off frequency is above 10MHz and is superior with respect to the other assembly techniques. Subsequent sections will focus on an experimental demonstration of 2D monolithic device.

Integration	Wire-bonding	TSVs	3D interconnect and direct metal-oxyde bonding	Monolithic
Cut-off frequency	~10kHz	~1MHz	~10MHz	~10MHz

Table II.10: Cut-off frequencies of different integration techniques.

II. NEMS-CMOS modelling

This section focuses on the design and modeling of NEMS-CMOS devices. The electromechanical device studied here after is based on an electrostatic actuation and a capacitive transduction (called detection as well), such as illustrated in Figure II.2.1.

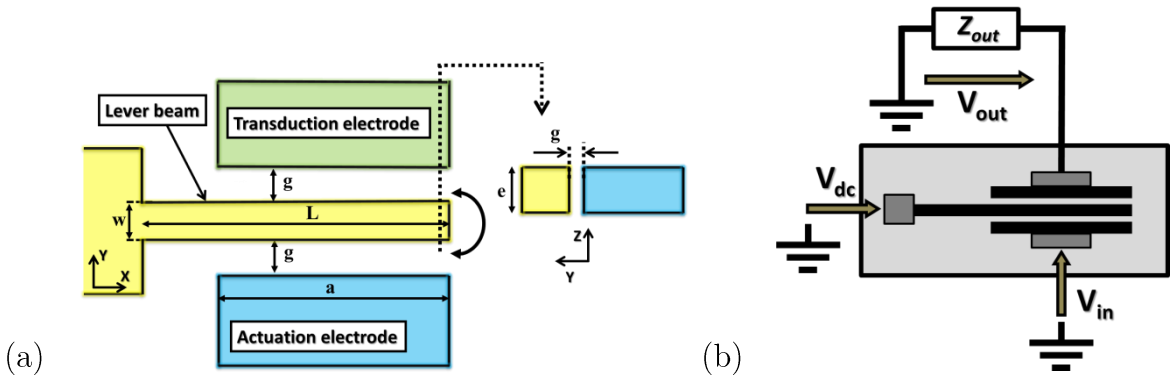


Figure II.2.1: Schematic representation (a) and electrical set-up (b) of a 3-ports NEMS resonator structure based on a clamped-free beam.

II.1 Device description and electromechanical model

As described in section II.2 of the first chapter, NEMS resonators comprise three different stages, depicted as three block diagrams in Figure II.2.2: an actuation stage, a resonating element and a transduction part.

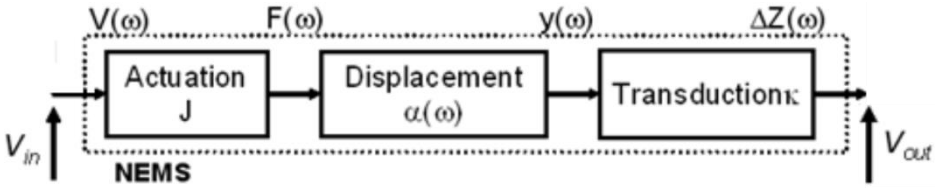


Figure II.2.2: Block diagram representation of a NEMS resonator [Col09].

II.1.1 – Actuation

The actuation of a resonator device is used to set into motion a movable structure (a lever beam in Figure II.2.1). It converts an input signal V_{in} which can have diverse physical origin (optic, magnetic, thermo-elastic etc.) into a force F applied on the structure. The nano-resonator studied in this thesis uses an electrostatic actuation

to move the beam. The induced electrostatic force F can be expressed considering the beam and the actuation electrode as capacitor plates storing an electrostatic energy U:

$$F = -\frac{\partial U}{\partial y} = -\frac{1}{2}\frac{\partial C}{\partial y}\Delta V^2 \ \text{[N]} \tag{II.24}$$

where ΔV and C respectively correspond to the voltage difference and the capacitance between the movable cantilever and the actuation electrode whereas y is the beam displacement. From Figure II.2.1 (a), the capacitance and its first derivative can be determined.

$$C = \frac{\varepsilon_0 e a}{g - y} \ \text{[F]} \qquad \text{if y>0} \tag{II.25}$$

$$\frac{\partial C}{\partial y} = \frac{\varepsilon_0 e a}{g^2 \cdot \left(1 - \frac{y}{g}\right)^2} \ \text{[F.m}^{-1}\text{]} \tag{II.26}$$

e corresponds to the beam thickness, a the actuation electrode length and g to the gap between the beam and the actuation electrode. Within the limit of small deflections compared to the gap, (II.26) becomes:

$$\frac{\partial C}{\partial y} \approx \frac{\varepsilon_0 e a}{g^2} \tag{II.27}$$

Figure II.2.1 (b) shows that two different voltages are applied on the system: a dc-voltage V_{dc} on the cantilever and an ac-voltage V_{in} on the actuation voltage. The latter is expressed below:

$$V_{in}(\omega) = V_{in-ac} \cdot \cos(\omega t) \tag{II.28}$$

Therefore, by combining (II.24), (II.27) and (II.28), the expression of Fcan be determined:

$$F(\omega) \approx \frac{\varepsilon_0 e a}{2g^2}\left(V_{in-ac}\cos(\omega t) - V_{dc}\right)^2 \tag{II.29}$$

$$F(\omega) \approx \frac{\varepsilon_0 e a}{2g^2}\left(\underbrace{V_{dc}^2 + \frac{V_{in-ac}^2}{2}}_{A} - \underbrace{2V_{dc}V_{in-ac}\cos(\omega t)}_{B(\omega)} + \underbrace{\frac{V_{in-ac}^2}{2}\cos(2\omega t)}_{C(2\omega)}\right) \tag{II.30}$$

The electrostatic force has three components according to (II.30): one dc term (A), one so-called "one-ω" term (B) and a last one so-called "two-ω" term (C). Since the samples are electrically characterized using a direct method (called homodyne as well), only the "one-ω" signal component is studied. Consequently, the voltages V_{dc} and $V_{in\text{-}ac}$ are required. In practice, $V_{in\text{-}ac}$ is generally much smaller than V_{dc}. (II.30) thereby becomes:

$$F(\omega) \approx \frac{\varepsilon_0 e a}{2g^2}\left(\underbrace{V_{dc}^2}_{A} - \underbrace{2V_{dc}V_{in-ac}\cos(\omega t)}_{B(\omega)} \right) \tag{II.31}$$

An actuation gain J can be defined as the ratio of the ac component of the electrostatic force over the input signal voltage, as indicated in Figure II.2.2.

$$J = \frac{F(\omega)}{V_{in}(\omega)} = \frac{\varepsilon_0 e a}{g^2} V_{dc} \ [\mathrm{N.V^{-1}}] \tag{II.32}$$

II.1.2 – NEMS dynamics

The transfer function $\alpha(\omega)$ between the actuation force and the resulting mechanical displacement is obtained from the Euler-Bernouilli equation usually solved using Galerkin procedure[14]. An equivalent lumped model represents the resonating cantilever as a driven damped mass-spring system with a mass m (in kg), a stiffness coefficient k (in $\mathrm{N.m^{-1}}$) and a damping coefficient c (in $\mathrm{N.m^{-2}}$) on which a force F_{act} is applied, as illustrated in Figure II.2.3. This system is considered as linear, *i.e.* the displacement amplitude of the beam is small enough with respect to the gap g and to the critical amplitude which is at the onset of nonlinearity [Mil10-Kac09]. The mass m is subjected to the electrostatic actuation force F_{act}. The fundamental principle of dynamics applied on the mass gives:

$$m\ddot{y} = F_{act} - c\dot{y} - ky \tag{II.33}$$

[14] More information is provided in [Arn11] and [Mil10].

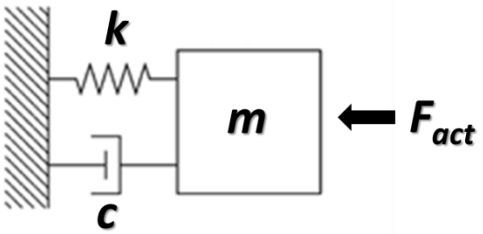


Figure II.2.3: Damped mass-spring system used to model the resonating cantilever.

y and F_{act} are expressed with complex numbers where ω represents the pulsation of the actuation force.

$$y(\omega) = Y_0 \cdot e^{j\omega t} \tag{II.34}$$

$$F_{act}(\omega) = F_0 \cdot e^{j\omega t} \tag{II.35}$$

Equation (II.33) thereby becomes:

$$-m\omega^2 y(\omega) = F_{act}(\omega) - c\omega \cdot y(\omega) - k y(\omega) \tag{II.36}$$

The transfer function $\alpha(\omega)$is then:

$$\alpha(\omega) = \frac{y(\omega)}{F_{act}(\omega)} = \frac{1}{-m\omega^2 + jc\omega + k} = \frac{\frac{1}{k}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \quad [\mathrm{m.N^{-1}}] \tag{II.37}$$

$$\text{with } \omega_0 = \sqrt{\frac{k}{m}} \quad [\mathrm{rad.s^{-1}}] \tag{II.38}$$

$$\text{and } Q = \frac{\sqrt{k \cdot m}}{c} \tag{II.39}$$

ω_0 and Q are respectively the mechanical resonance pulsation of the first mode and the quality factor of this resonance mode. This last parameter can be understood as the ratio of the total elastic energy stored in one vibration cycle over the dissipated energy during this same cycle. This dissipation has various origins such as the viscous damping of the surrounding fluid, losses at the beam anchor, thermo-elastic, surface and volume-related losses [Kac10].

Following the Euler-Bernoulli approach, the resonance pulsation, the effective beam stiffness and the effective mass of the nano-resonator can be determined according to the cantilever dimensions and the material properties [Arn11].

$$\omega_0 = 1.015\sqrt{\frac{E}{\rho}}\frac{w}{L^2} \tag{II.40}$$

$$k_{eff} = 0.658\frac{Ew^3e}{L^3} \tag{II.41}$$

$$m_{eff} = 0.639\rho \cdot Lwe \tag{II.42}$$

E and ρ respectively correspond to the Young modulus (in Pa) and the density (in kg.m^{-3}) of the resonator material. Both k_{eff} and m_{eff} are calculated with respect to the maximum vibration amplitude point.

II.1.3 – Transduction

The transduction part converts the mechanical displacement y of the cantilever into an electrical signal through the motion-induced change of the beam-electrode capacitance (see Figure II.2.1). Considering small displacements with respect to the gap, the transduction gain κ corresponding to the ratio of the capacitance variation δC over the mechanical displacement is:

$$\kappa = \frac{\delta C(\omega)}{y(\omega)} \approx \frac{\varepsilon_0 ea}{g^2} \text{ [F.m}^{-1}\text{]} \tag{II.43}$$

II.1.4 – Signal transmission between the NEMS device and an external apparatus

In order to complete the NEMS transfer function, the signal transmission between the transduction and the output impedance Z_{out} must be investigated. As depicted in Figure II.2.4, this impedance will be symbolized by a capacitance C_{out} representing connection capacitances and typical input of a measurement apparatus.

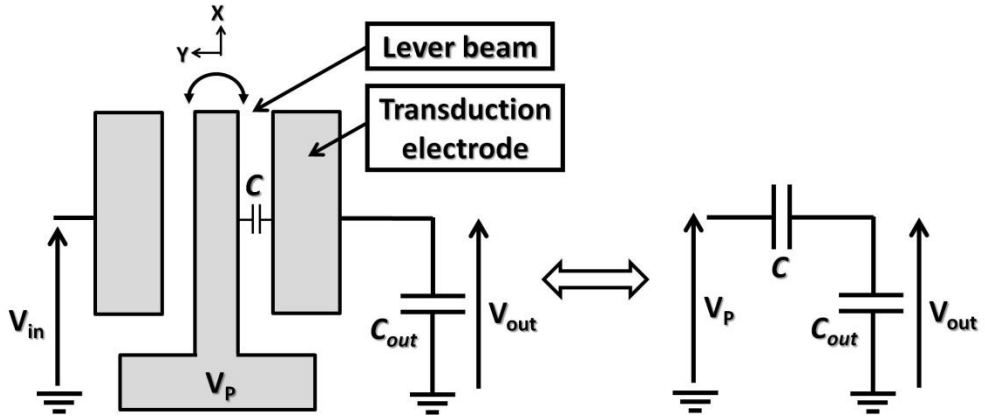


Figure II.2.4: Schematic illustration and equivalent electrical representation of a NEMS resonator with capacitive detection connected to an output capacitance.

From this electrical representation, the transfer function R can be calculated.

$$R = \frac{v_{out}}{\delta C} \ [\mathrm{V.F^{-1}}] \tag{II.44}$$

$$\frac{V_{out}}{V_P} = \frac{1/jC_{out}\omega}{1/jC_{out}\omega + 1/jC\omega} = \frac{C}{C + C_{out}} \tag{II.45}$$

Expression (II.45) can be turned into (II.46):

$$(C + C_{out}) \cdot V_{out} = C \cdot V_P \tag{II.46}$$

Finding R imposes to differentiate this last expression with respect to the time and to work with ac-signals. Consequently, y and V_{out} are written in complex form.

$$y(\omega) = Y_0 \cdot e^{j\omega t} \text{ and } V_{out}(\omega) = V_{out-dc} + v_{out-ac} \cdot e^{j\omega t} \quad \text{with} \quad V_{out-dc} >> v_{out-ac} \tag{II.47}$$

As V_P corresponds to a dc-voltage, the derivative differentiation of (II.46) gives:

$$V_{out-dc}\frac{\partial C}{\partial t} + (C + C_{out})\frac{\partial V_{out}}{\partial t} = V_P \frac{\partial C}{\partial t} \tag{II.48}$$

$$V_{out-dc}\frac{\partial C}{\partial y}\frac{\partial y}{\partial t} + (C + C_{out})\frac{\partial V_{out}}{\partial t} = V_P \frac{\partial C}{\partial y}\frac{\partial y}{\partial t} \tag{II.49}$$

$$V_{out-dc}\frac{\partial C}{\partial y} \cdot j\omega \cdot y + (C + C_{out}) \cdot j\omega \cdot v_{out-ac} = V_P \frac{\partial C}{\partial y} j\omega \cdot y \tag{II.50}$$

Considering small displacements from the NEMS resonator, y can be assimilated as ∂y; leading thus to (II.51) and (II.52).

$$V_{out-dc} \cdot \delta C + (C + C_{out}) \cdot v_{out-ac} = V_P \cdot \delta C \tag{II.51}$$

$$R = \frac{v_{out-ac}}{\delta C} \approx \frac{V_P - V_{out-dc}}{C + C_{out}} \tag{II.52}$$

II.1.5 – Overall response of the system

The global NEMS transfer function $H_{NEMS}$is then:

$$H_{NEMS}(\omega) = \frac{V_{out}}{V_{in}}(\omega) = \frac{V_{out}}{\delta C}(\omega) \cdot \frac{\delta C}{y}(\omega) \cdot \frac{y}{F}(\omega) \cdot \frac{F}{V_{in}}(\omega) = R \cdot \kappa \cdot \alpha(\omega) \cdot J \tag{II.53}$$

Consequently:
$$H_{NEMS}(\omega) = \frac{G_{NEMS}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \tag{II.54}$$

with
$$G_{NEMS} \approx \frac{\varepsilon_0^2 e^2 a^2 V_{dc}(V_{dc} - V_{out-dc})}{g^4 k_{eff}(C + C_{out})} \tag{II.55}$$

II.2 Equivalent electrical model presentation

Another approach consists in modelling the NEMS resonator as an electrical component. Two representations are used to analyze the resonator features and performances through its transfer function $H_{res}(\omega)$.

The Bode diagram depicts the gain $G(\omega)$ (or $G_{dB}(\omega)$ in dB) and the phase-shift $\varphi(\omega)$ evolution with respect to the pulsation ω, as defined below.

$$G_{res}(\omega) = |H_{res}(\omega)| \qquad G_{res-dB}(\omega) = 20 \cdot \log_{10}[|H_{res}(\omega)|] \text{ [dB]} \tag{II.56}$$

$$\varphi_{res}(\omega) = \arg(H_{res}(\omega)) \text{ [rad]} \tag{II.57}$$

The Nyquist diagram represents the imaginary part (so-called quadrature signal) $Y(\omega)$ with respect to its real part (so-called in-phase component) $X(\omega)$ of $H_{res}(\omega)$ in function of the pulsation.

$$X_{res}(\omega) = real(H_{res}(\omega)) \tag{II.58}$$

$$Y_{res}(\omega) = imag(H_{res}(\omega)) \tag{II.59}$$

These two representations are linked each other by (II.60).

$$X_{res}(\omega) = G_{res}(\omega)\cdot\cos(\varphi_{res}(\omega)) \qquad Y_{res}(\omega) = G_{res}(\omega)\cdot\sin(\varphi_{res}(\omega)) \tag{II.60}$$

A RLC circuit is usually used to electrically represent a resonator. As illustrated in Figure II.2.5, two contributions can be identified. One comes from the motion of the beam and is characterized by its motional impedance Z_M formed by a series resistance R_M with an inductance L_M and a capacitance C_M. The expression of Z_M is given in (II.61).

$$Z_M(\omega) = R_M + jL_M\omega + \frac{1}{jC_M\omega} = \frac{jR_MC_M\omega - L_MC_M\omega^2 + 1}{jC_M\omega} \ [\Omega] \tag{II.61}$$

In addition, an input-to-output parasitic signal, so-called feedthrough signal, is also present. This contribution is not included in the transfer function depicted in (II.61). This feedthrough part, characterized by its impedance Z_{ft}, may come from many sources, such as the NEMS intrinsic capacitance, fringing field effects or parasitic coupling (for instance through the substrate) [Lee09-Arc10].

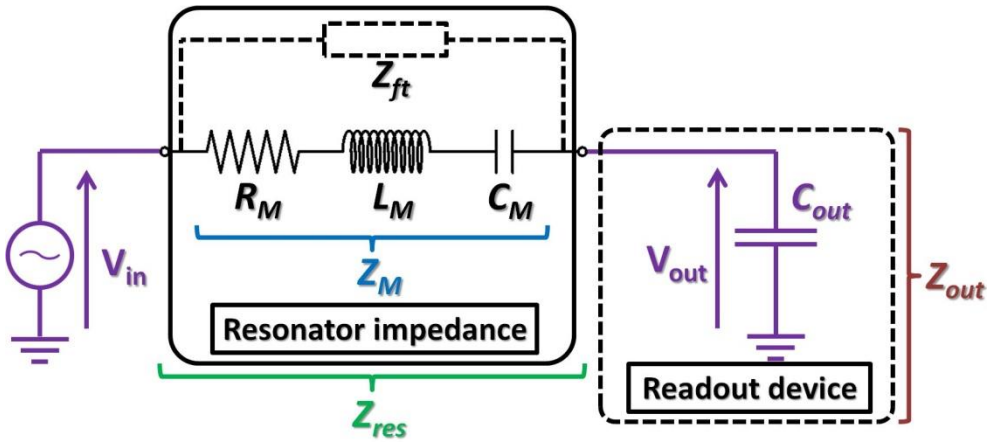


Figure II.2.5: Electrical representation of a NEMS resonator in an open-loop configuration.

Considering the electrical schematic of Figure II.2.5, the resonator impedance is

$$Z_{res}(\omega) = \frac{1}{\frac{1}{Z_M(\omega)} + \frac{1}{Z_{ft}(\omega)}} \ [\Omega] \tag{II.62}$$

According to the configuration from Figure II.2.5, $H_{res}(\omega)$ can be calculated.

$$H_{res}(\omega) = \frac{V_{out}}{V_{in}}(\omega) = \frac{Z_{out}(\omega)}{Z_{out}(\omega) + Z_{res(\omega)}} = \frac{\frac{1}{jC_{out}\omega}}{\frac{1}{jC_{out}\omega} + Z_{res}(\omega)} \tag{II.63}$$

Assuming that readout input impedance $Z_{out}(\omega)$ can be neglected compared to $Z_{res}(\omega)$, expression (II.63) becomes:

$$H_{res}(\omega) \approx \frac{1}{jC_{out}Z_{res}(\omega)\cdot\omega} \approx \frac{1}{jC_{out}\omega}\cdot\left(\frac{1}{Z_M(\omega)} + \frac{1}{Z_{ft}}\right) \tag{II.64}$$

The development of (II.64) in (II.65) shows that $H_{res}(\omega)$ is composed by two terms: $H_{NEMS}(\omega)$ and $H_{ft}(\omega)$ respectively corresponding to the nano-resonator and the feedthrough transfer function.

$$H_{res}(\omega) \approx \frac{\frac{C_M}{C_{out}}}{\underbrace{1 - L_M C_M \omega^2 + jR_M C_M \omega}_{H_{NEMS}(\omega)}} + \underbrace{\frac{1}{jC_{out}Z_{ft}\omega}}_{H_{ft}(\omega)} \tag{II.65}$$

For simplification, $H_{NEMS}(\omega)$ is rewritten according to (II.66)

$$H_{NEMS}(\omega) = \frac{G_{NEMS}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \tag{II.66}$$

$$\omega_0 = \sqrt{\frac{1}{L_M C_M}} \tag{II.67}$$

$$Q = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} \tag{II.68}$$

$$G_{NEMS} = \frac{C_M}{C_{out}} \tag{II.69}$$

By comparing the mechanical with the electrical models and associating (II.38), (II.39), (II.55) with (II.67), (II.68) and (II.69), R_M, L_M and C_M expressions can be determined.

$$C_M = \frac{QC_{out}\eta^2 V_{dc}\left(V_{dc} - V_{out-dc}\right)}{k \cdot \left(\frac{\varepsilon_0 ea}{g} + C_{out}\right)} \text{ [F]} \tag{II.70}$$

$$L_M = \frac{m\left(\frac{\varepsilon_0 ea}{g} + C_{out}\right)}{C_{out}\eta^2 V_{dc}\left(V_{dc} - V_{out+dc}\right)} \text{ [H]} \tag{II.71}$$

$$R_M = \frac{\sqrt{km}}{Q} \cdot \frac{\frac{\varepsilon_0 ea}{g} + C_{out}}{C_{out}\eta^2 V_{dc}\left(V_{dc} - V_{out-dc}\right)} \text{ [}\Omega\text{]} \tag{II.72}$$

$$\text{with } \eta = \frac{\varepsilon_0 ea}{g^2} \text{ [F.m}^{-1}\text{]} \tag{II.73}$$

More details about $Z_{ft}(\omega)$will be provided in the next section.

II.3 Theoretical study

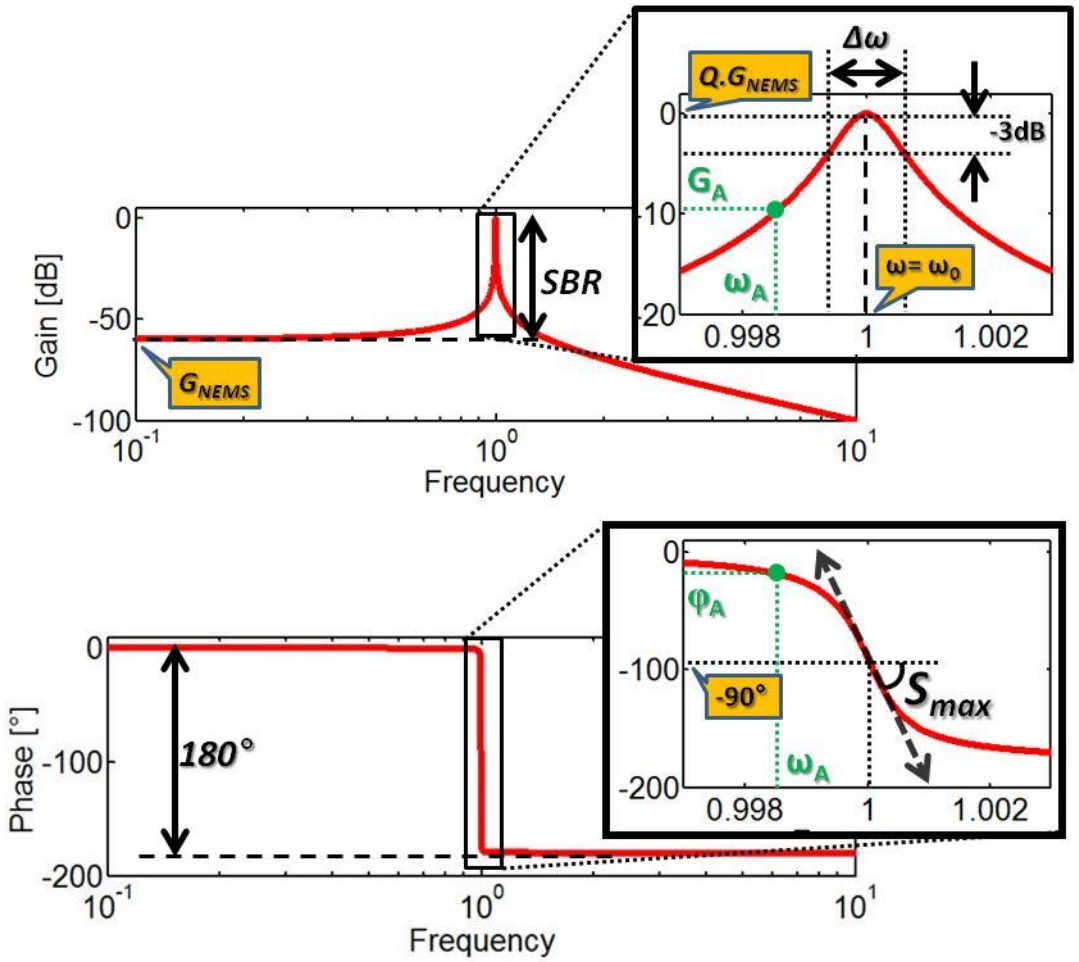
As said before, both Bode and Nyquist diagrams can be used to describe any resonator performance. Thanks to (II.60), one of the representations can be switched to the other one. This specifity is represented on Figure II.2.6 through the point M(ω_A) with (G_A; φ_A) and (X_A;Y_A) as coordinates respectively in the Bode and the Nyquist representation.

Through the theoretical study of the NEMS frequency response, some important notions relative to the resonators can be explained. Some of these parameters are necessary for modelling the system and for the determination of the sensor performances. Figure II.2.6 depicts a typical Bode (a) and Nyquist (b) diagram of nano-resonator with a gain G_{NEMS} and a quality factor Q respectively equal to 1.10^{-3} and 1.10^{3}. In a first time, the feedthrough contribution is neglected with respect to the NEMS response. $Z_{res}(\omega)$ thereby corresponds to the NEMS motional impedance Z_M:

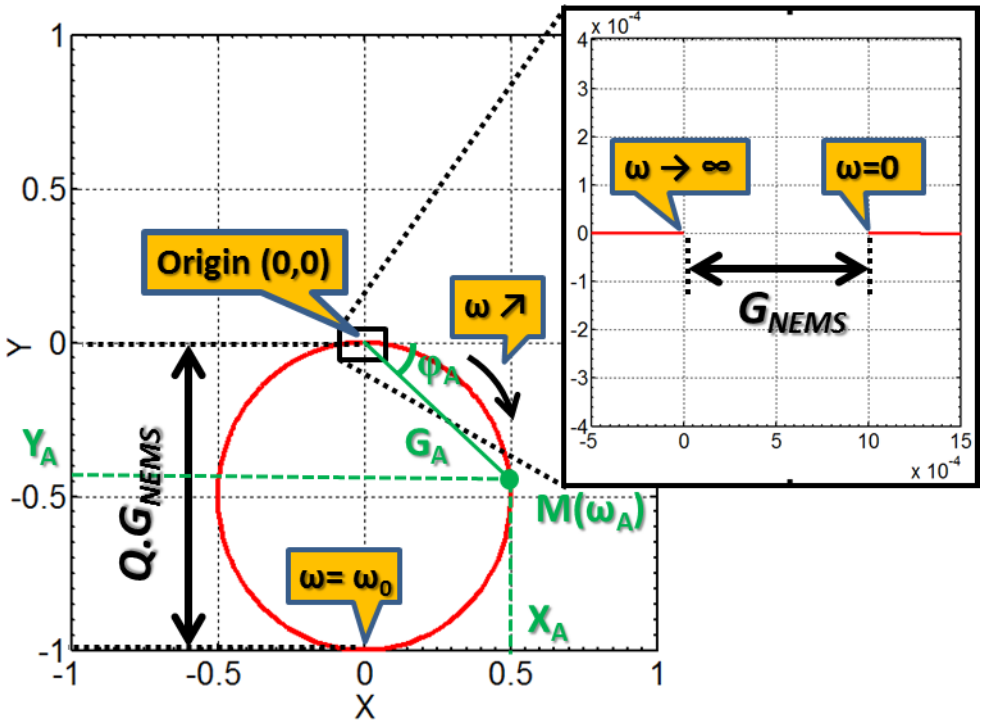
$$Z_{res}(\omega) = Z_M(\omega) \tag{II.74}$$

Therefore:

$$H_{res}(\omega) \approx H_{NEMS}(\omega) \tag{II.75}$$



(a)



(b)

Figure II.2.6: Bode (a) and Nyquist diagrams (b) of a resonator with a weak feedthrough contribution. The insets in (a) and (b) correspond to zooms of the frequency response near the resonance. G_{NEMS} and Q are respectively set at 10^{-3} and 10^{3}.

The main characteristic parameters are explained below and illustrated in Figure II.2.6.

- The resonance frequency f_{res} (or pulsation ω_{res}) is characterized by different features described in the different equations below. Moreover, the gain $G_{res}$and the phase-shift slope S achieve their maximum value (II.77) and (II.78) for a large quality factor. Considering a negligible feedthrough signal, f_{res} corresponds to the mechanical resonance frequency f_0 of the resonator as observed in (II.77) and (II.78). At this frequency, the phase-shift is equal to -90° (II.79).

$$G_{res}(\omega)=\frac{G_{NEMS}}{\sqrt{\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)^2+\left(\frac{\omega}{\omega_0 Q}\right)^2}} \text{ and } \varphi_{res}(\omega)=-\tan^{-1}\left(\frac{\frac{\omega}{\omega_0 Q}}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right) \quad \text{(II.76)}$$

$$\frac{\partial G_{res}}{\partial \omega}=0 \Rightarrow \frac{\omega}{\omega_0}=\frac{\sqrt{2}}{2}\cdot\sqrt{\frac{2Q^2+1}{Q^2}} \approx 1 \text{ for Q>>1} \quad \text{(II.77)}$$

$$\frac{\partial^2 \varphi}{\partial^2 \omega}=\frac{\partial S}{\partial \omega}=0 \Rightarrow \frac{\omega}{\omega_0}=\sqrt{-1+\frac{1}{Q}\sqrt{4Q^2-1}} \approx 1 \text{ for Q>>1} \quad \text{(II.78)}$$

$$\varphi_{res}(\omega_0)=-90° \quad \text{and} \quad G_{res}(\omega_0)=QG_{NEMS} \quad \text{(II.79)}$$

- The quality factor Q, defined in (II.80) and illustrated in the inset of Figure II.2.6 (a), is electrically defined as the ratio of the resonance frequency f_{res} (or pulsation ω_{res}) over the bandwidth Δf (or $\Delta\omega$) at -3dB (II.80). The latter is defined in (II.81).

$$Q=\frac{f_{res}}{\Delta f}=\frac{\omega_{res}}{\Delta\omega} \quad \text{(II.80)}$$

$$G_{res}(f_{res}\pm\Delta f)=\frac{G_{res}(f_{res})}{\sqrt{2}} \Leftrightarrow G_{res-dB}(f_{res}\pm\Delta f)=G_{res-dB}(f_{res})-3dB \quad \text{(II.81)}$$

- The phase sensitivity S of a resonator corresponds to the slope of the phase-shift with respect to the frequency. The latter achieves its maximum value at the resonance frequency according to (II.78). The value of sensitivity is given in (II.82).

$$S(\omega)=\frac{\partial\varphi}{\partial\omega}\,[\text{rad.s}^{-1}] \Leftrightarrow S(f)=\frac{\partial\varphi}{\partial f}\,[\text{rad.Hz}^{-1}] \quad \text{and} \quad S_{\max}\approx|S(\omega_0)|=\frac{2Q}{f_0} \tag{II.82}$$

- The Signal-to-Background ratio SBR corresponds to the ratio of the total signal V_{res}(*i.e.* NEMS and feedthrough) over the feedthrough signal V_{ft}, as defined in (II.83). This SBR can also be given by the ratio of the resonator gain (G_{res}) over the feedthrough gain (G_{ft}). In practice, this ratio is generally determined at the resonance frequency.

$$SBR(\omega)=\frac{V_{res}(\omega)}{V_{ft}(\omega)}=\frac{G_{res}(\omega)}{G_{ft}(\omega)} \tag{II.83}$$

All these parameters can be determined by analyzing the resonators frequency response through Bode and Nyquist diagrams, as indicated in Figure II.2.6. The latter represents the frequency response of the system with respect to the normalized frequency f/f_0 (equivalent to the ω/ω_0 ratio). The Bode diagram shows the presence of a resonance peak for the gain at the frequency f_0 and a 180° phase-shift before and after resonance. The Nyquist representation depicts a circle with a diameter equal to $Q.G_{NEMS}$ which characterizes the NEMS frequency response. On this circle, the farthest point with respect to the origin corresponds to the resonance of the system.

The objective is to obtain a low feedthrough signal in order to maximize the sensitivity of the resonator which is affected by the feedthrough parasitic signal. Its effect on the sensor characteristic will now be investigated.

(II.84) reminds the expression of the feedthrough transfer function H_{ft}:

$$H_{ft}(\omega)=\frac{1}{jC_{out}Z_{ft}\omega} \tag{II.84}$$

Most of the time, Z_{ft}can be modelled as a parasitic capacitance C_{ft}. H_{ft} thereby becomes constant and does not vary with ωas shown in (II.85), leading to the new expression of $H_{res}(\omega)$ expressed in (II.86).

$$H_{ft} = \frac{C_{ft}}{C_{out}} \tag{II.85}$$

$$H_{res}(\omega) \approx \frac{G_{NEMS}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} + H_{ft} \tag{II.86}$$

This feedthrough affects the frequency response of the system. As observed on the Bode diagram of Figure II.2.7, another peak so-called anti-resonance peak appears in the gain response. At these resonance and anti-resonance frequencies (respectively noted f_{res} and $f_{a\text{-}res}$), G_{res} respectively achieves its maximum and minimum value. These frequencies can be determined by solving equation (II.87). As depicted on Figure II.2.8, the resonance frequency f_{res} is almost equal to f_0 for any value of the H_{ft}/G_{NEMS} ratio. However, the higher this ratio is, the closer the anti-resonance to the resonance peak is (see the blue curve of Figure II.2.8).

On the Nyquist diagram of Figure II.2.7, the NEMS resonator characteristic is not affected in shape but is only translated of a distance H_{ft} from the origin of the X-Y graph. The resonance noted $R(\omega_{res})$ and anti-resonance noted $AR(\omega_{a\text{-}res})$ respectively correspond to the farthest (*i.e.* the highest module noted G_{res}) and to the closest (*i.e.* the lowest module noted $G_{a\text{-}res}$) point on the circle with respect to the origin. These two points have the same phase-shift noted φ_{res}.

H_{ft} has also an incidence on the phase response. As H_{ft}/G_{NEMS} ratio gets higher, both total phase-shift $\Delta\varphi_{tot}$ and maximum slope S_{MAX} decrease, consequently affecting the resonator sensitivity as expressed in (II.88) and illustrated in Figure II.2.8. $S_{MAX\text{-}red}$, defined in (II.89), corresponds to the normalized sensitivity with respect to the resonance pulsation.

$$\frac{\partial G_{res}}{\partial \omega}(\omega) = 0 \Leftrightarrow \begin{cases} \omega = \omega_{res} = \omega_0 \sqrt{1 + \frac{G_{NEMS}}{2H_{ft}} - \frac{1}{2Q}\sqrt{Q^2\left(\frac{G_{NEMS}}{H_{ft}}\right)^2 + 2\frac{G_{NEMS}}{H_{ft}} + 4}} \\ \omega = \omega_{a-res} = \omega_0 \sqrt{1 + \frac{G_{NEMS}}{2H_{ft}} + \frac{1}{2Q}\sqrt{Q^2\left(\frac{G_{NEMS}}{H_{ft}}\right)^2 + 2\frac{G_{NEMS}}{H_{ft}} + 4}} \end{cases} \tag{II.87}$$

$$S_{MAX} \approx |S(\omega_{res})| = \left| \frac{Q\frac{G_{NEMS}}{H_{ft}}\left(1 - 2Q^2\frac{G_{NEMS}}{H_{ft}}\right)}{\left(1 + Q^2\frac{G_{NEMS}^2}{H_{ft}^2}\right)\omega_{res}} \right| \tag{II.88}$$

$$S_{MAX-red} = \frac{\partial \varphi}{\partial \upsilon} = \left| \frac{Q\frac{G_{NEMS}}{H_{ft}}\left(1 - 2Q^2\frac{G_{NEMS}}{H_{ft}}\right)}{\left(1 + Q^2\frac{G_{NEMS}^2}{H_{ft}^2}\right)} \right| \text{where} \upsilon = \frac{\omega}{\omega_{res}} \tag{II.89}$$

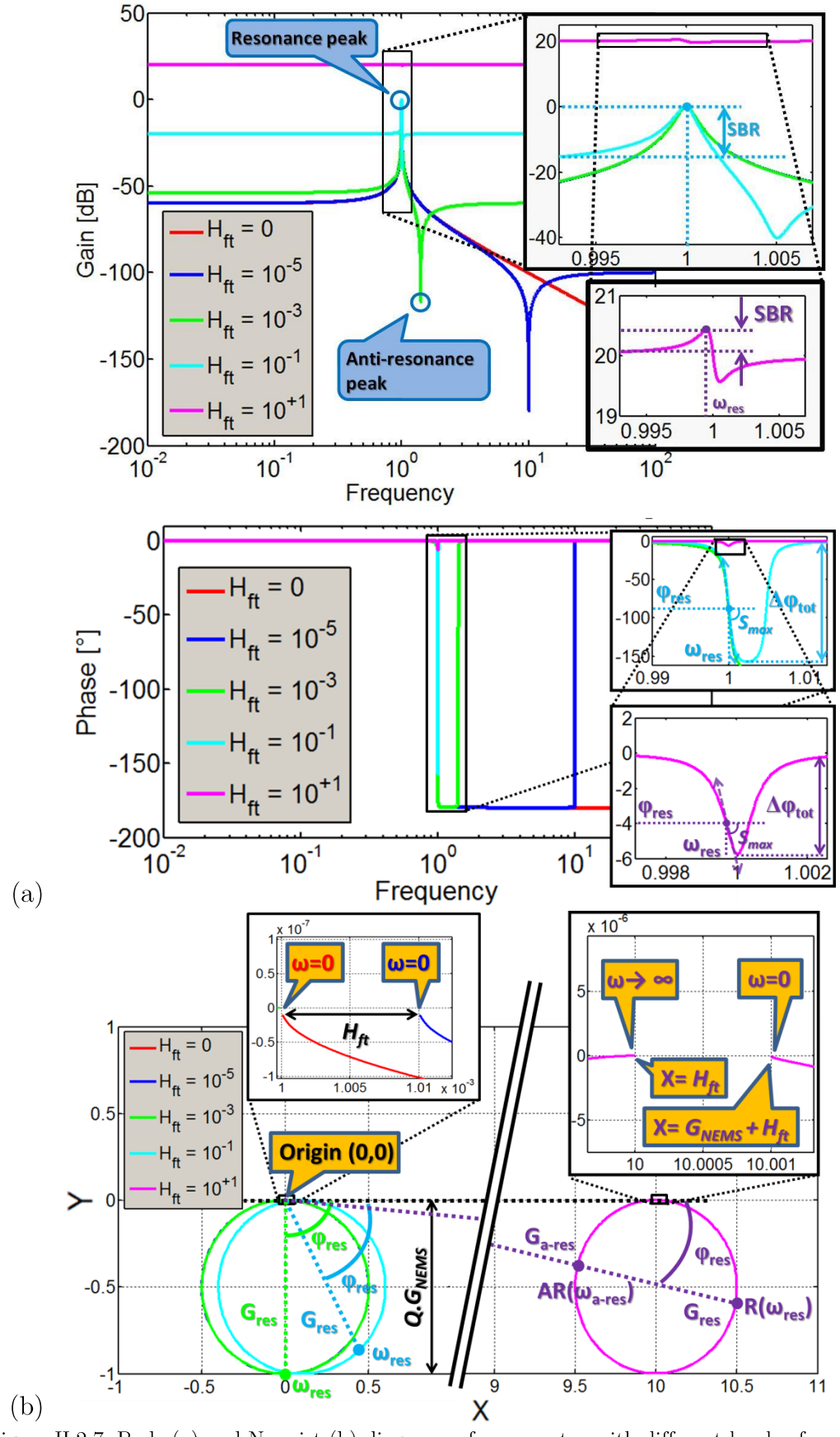


Figure II.2.7: Bode (a) and Nyquist (b) diagrams of a resonator with different levels of capacitive feedthrough. The insets in (a) and (b) correspond to different zooms of the frequency response near the resonance frequency. G_{NEMS} and Q are respectively set at 10^{-3} and 10^{3}.

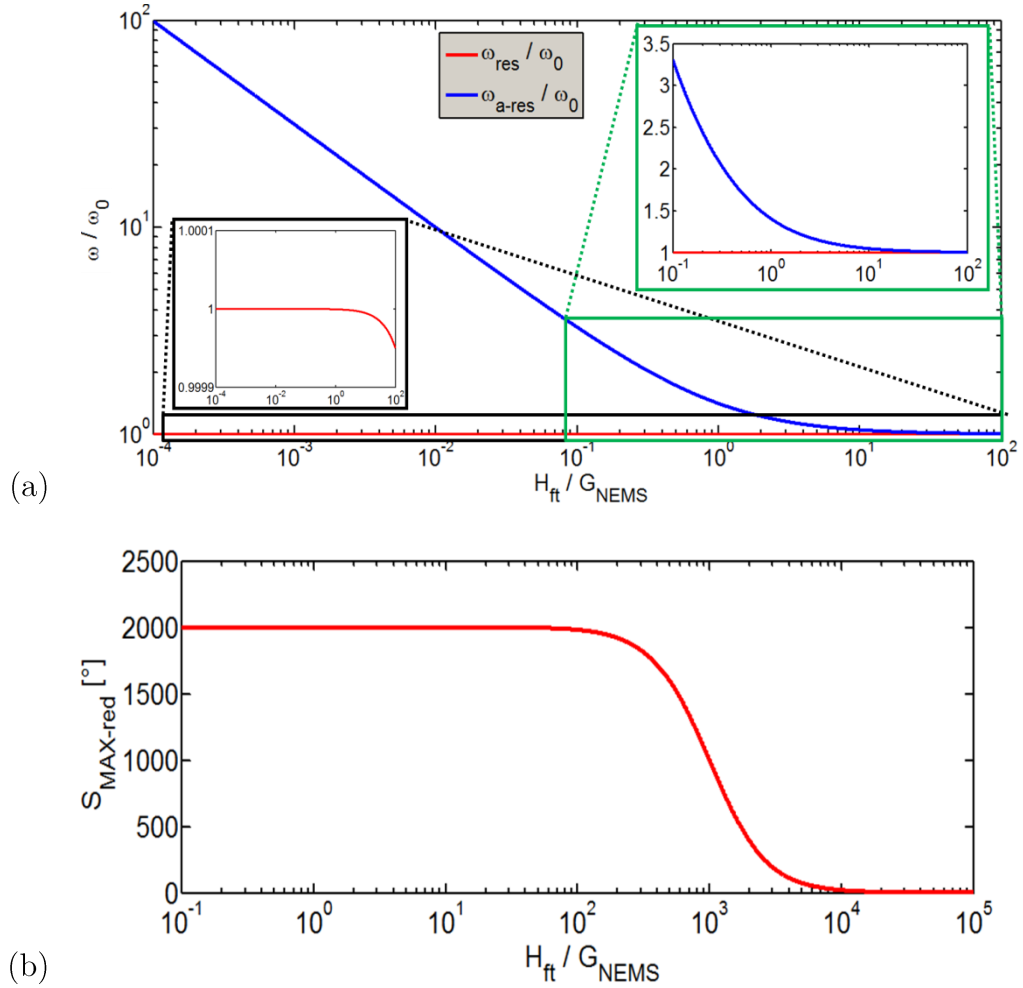


Figure II.2.8: Variation of both resonance and anti-resonance pulsations (a) and variation of the sensitivity (b) with respect to the H_{ft}/G_{NEMS} ratio.

As described in chapter I, the mass detection is performed by tracking each resonance frequency variation Δfover time. Considering an open-loop configuration, an accurate way consists in measuring the phase-shiftvariation $\Delta\varphi$ in order to detect any frequency modification due to a mass deposition [Arn11]. All these elements are linked with the sensitivity S according to (II.90).

$$\Delta\varphi = \frac{\partial\varphi}{\partial f}\Delta f = S \cdot \Delta f \tag{II.90}$$

(II.82) and (II.88) show that maximum sensitivity is obtained at the resonance frequency f_{res}. This parameter also depends on the feedthrough effect (see Figure II.2.8-(b)) which has to be minimized with respect to the gain achieved at the resonance. Some solutions exist to reduce this parasitic effect, such as heterodyne or downmixing detection techniques [Bar05].

Another important parameter concerns the frequency resolution directly linked to the mass resolution (II.91). M_{res} corresponds to the effective mass of the resonator, whereas $\sigma_{\delta f}$ and σ_m are the frequency and the mass resolution of the device.

$$\sigma_m = \frac{2M_{res}}{f_{res}}\sigma_{\delta f} \text{ [kg]} \tag{II.91}$$

A high value of f_{res} and a low value of $\sigma_{\delta f}$ provide a low mass resolution necessary for the mass detection application. In an open-loop configuration, the frequency resolution is determined from the phase-shift measurements near the resonance frequency (see Figure II.2.9). For different acquisition times T_{meas} and with a lock-in amplifier (refer to [Sag13] and [Arn11]), X_{res} and Y_{res} parts (defined in (II.58), (II.59) and (II.60)) are measured. X_{res} and Y_{res} are both linked to the phase-shift (II.92).

$$\tan\left[-\frac{\pi}{2} - \varphi_{res}(\omega)\right] = \frac{X_{res}}{Y_{res}} \tag{II.92}$$

As $\varphi_{res}(\omega)$ is close to $-\pi/2$ during the measurement near the resonance, the phase deviation noted $\Delta\varphi_{res}$ can be expressed according to (II.93) where X_{noise} corresponds to the in-phase signal noise and Y_{mean} the mean value of the quadratic component. The ratio of X_{noise} over Y_{mean} is linked to the signal-to-noise ratio (so called SNR). Moreover, from expression (II.90), the relative frequency deviation $\sigma_{\delta f}$ is linked to the SNR, expressed in (II.91).

$$\Delta\varphi_{res}(T_{meas}) = \frac{X_{noise}(T_{meas})}{Y_{mean}(T_{meas})} = \frac{1}{SNR} \tag{II.93}$$

$$\sigma_{\delta f} = \frac{1}{S_{\max} \cdot SNR} \text{ [Hz]} \tag{II.94}$$

Combining (II.91) with (II.94) leads to:

$$\sigma_m = \frac{2M_{res}}{f_{res} \cdot S_{\max} \cdot SNR} \text{ [kg]} \tag{II.95}$$

As a consequence, the sensitivity S_{max} constitutes a crucial parameter for mass detection performance, providing an easy detection of the frequency-shift (II.89), a better frequency noise [Rob82] and also a better mass resolution (II.95).

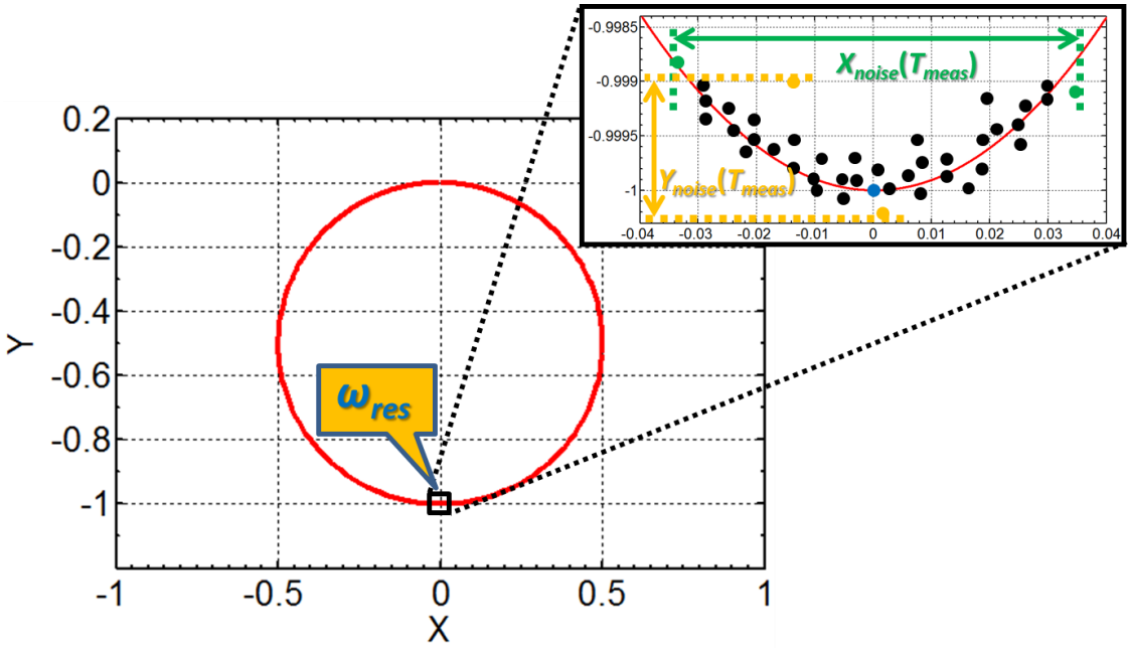


Figure II.2.9: Nyquist diagram of a NEMS resonator frequency response without feedthrough. The red curve is the theoretical characteristic. The blue point corresponds to the resonance; the black ones to the different measurement points near f_{res}, the green and yellow ones are respectively the extrema of both phase-shift and gain measurements during an acquisition time T_{meas}.

III. 2D NEMS-CMOS demonstrator study

Now the main theoretical parameters of NEMS resonators have been described, this section focuses on the experimental demonstration of a 2D capacitive NEMS-CMOS device and on the analysis of its electrical performances. In the scope of this thesis, its closed-loop operation is also demonstrated.

III.1 Fabrication process

The mechanical and electronic parts were performed on the same substrates. A pre-CMOS integration approach was used for this implementation. c-Si NEMS resonators are fabricated on the 1µm thick top-Si layer of SOI wafers (with 1µm thick BOX) prior to a standard 200mm 0.35µm 3.3V bulk CMOS technology from STMicroelectronics. In other words, a bulk CMOS technology is applied on SOI wafers without process modifications. The top Si layer is thick enough so that no change of transistor behavior is observed.

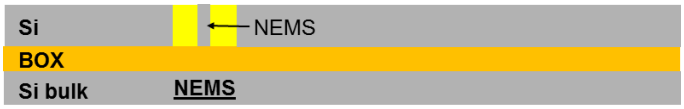
The process flow is depicted in Figure II.3.1 [Arc12]. It starts by the patterning of NEMS resonators in the top c-Si layer (with lateral dimensions down to 250nm and gaps in the same range), defined by 248nm DUV lithography and DRIE etching with a SiN/SiO_2 hard mask. Lateral trenches are performed to electrically isolate the different parts of the mechanical structures, and also the mechanical structures from the CMOS circuit that is fabricated later in the process. The lateral dimensions of the cavities used as NEMS detection gaps and as isolation trenches are limited to a few micrometers to later enable an effective filling with dielectric material. After filling these cavities with SiO_2, the wafers are planarized by chemical-mechanical polishing (CMP) (1).

At this point, the standard CMOS front-end process starts: formation of lateral isolating structures (LOCOS), MOS channels implantations, gate oxide formation, gate stack deposition and etching, spacers' formation, implantations of source/drain areas. Contacts on both NEMS and CMOS dedicated areas are subsequently formed by silicidation (2).

The back-end process is limited to the first metal level and its associated dielectric passivation (3). Then, in one step of dry etching, the back-end passivation layers are opened on top of NEMS areas and of contact pads in order to prepare the final release of the mechanical structures. A protective layer made up of HfO_2 is afterwards deposited all over the wafer surface (including the sidewalls of the openings in the passivation layers) in order to protect the CMOS circuits during the final release

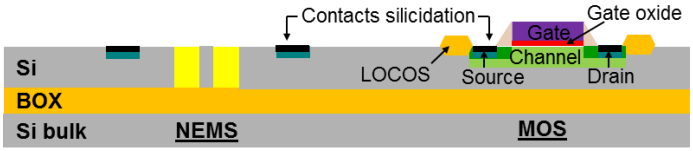
step (4). This layer is then patterned to enable the final release of the movable mechanical structures by vapor hydrofluoric acid (noted vapor HF) isotropic etching (5).

1



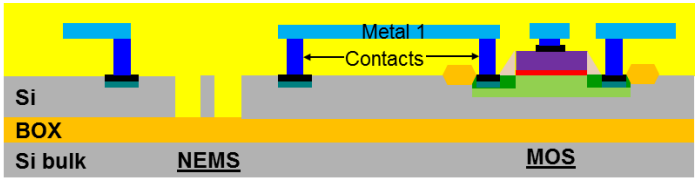
NEMS patterning, gaps filling and planarization.

2



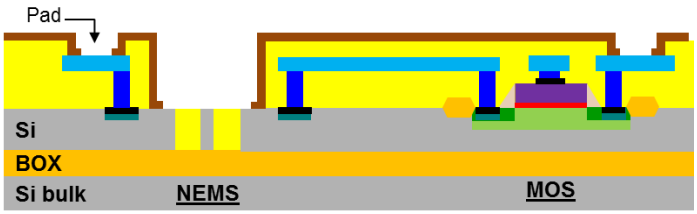
CMOS front-end process, doping and salicidation of MOS and NEMS contacts.

3



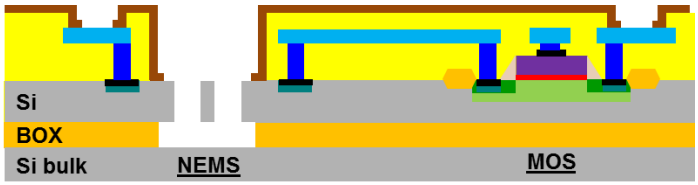
CMOS back-end process.

4



Back-end oxides opening followed by deposition and patterning of a protective layer (HfO_2 here).

5



NEMS release with vapor HF.

Figure II.3.1:NEMS-CMOS process flow(modified from [Arc12]).

III.2 Design of the demonstrator

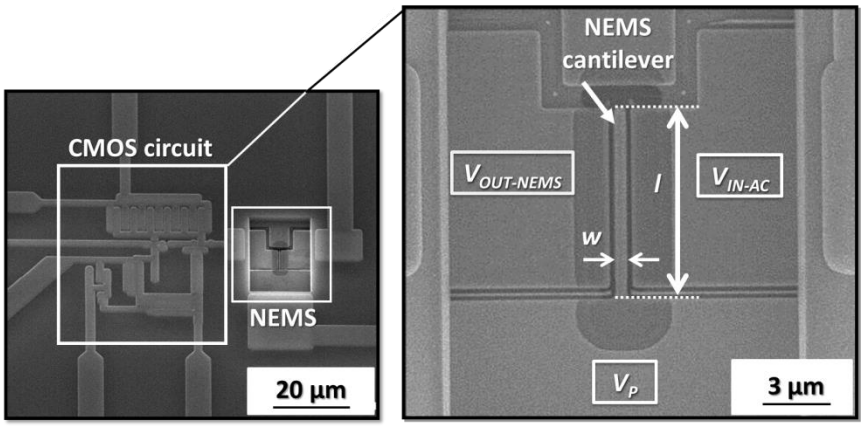


Figure II.3.2: SEM micrograph of the NEMS-CMOS device (left) with a zoom on the NEMS cantilever (right) with its electrodes and dimensions (l=8.3µm, w=0.5µm, g=0.25µm). l, w, g respectively correspond to the length, the width of the beam and the gap between the electrodes and the cantilever.

An SEM view is depicted in Figure II.3.2 with the mechanical beam dimensions. The nano-resonator uses an electrostatic actuation and a capacitive detection scheme. The movable part consists of a clamped-free beam. Six different designs were proposed for the cantilever dimensions and are depicted in Table II.11 with the resulting mechanical resonance frequency calculated from (II.40). The Young modulus E and density ρ are respectively 160 GPa and 2330 kg.m^{-3} and correspond to typical values for monocrystalline silicon.

The CMOS circuit provides both a suitable gain and phase-shift such that the Barkhausen conditions are fulfilled by the hybrid NEMS-CMOS system (see section III.4.3). This electronic circuit is monolithically linked to the mechanical part, thereby drastically decreasing the electrical signal losses at the beam output, as analyzed in the first part of this chapter. A very simple design was proposed for the CMOS part: seven transistors are used in two different blocks. An amplification stage provides the right gain and phase-shift just after the NEMS output while a unity gain buffer allows an impedance matching with external apparatus. The schematic of the whole system in a closed-loop configuration is presented in Figure II.3.3 (transistor dimensions are detailed in Table II.12). C_{01}, C_{02}, C_{OUT} and C_{PARA} are respectively the capacitances at the actuation and transduction part of the resonator, the capacitance present at the output of the amplification stage and the parasitic capacitance relative to the connection routing between NEMS and electronic circuit. Two types of cells were designed: some for open-loop operation, others for closed-loop, with the same NEMS resonators and circuit. The single difference is in the fact that the amplifier output is connected to the NEMS input which has no external actuation, *i.e.* no related contact pad.

NEMS device	PEL1P	PEL2P	PEL3P	PEL4P	PEL5P	PEL6P
l (µm)	5.9	8.3	8.3	11.7	4.1	5.9
w (µm)	0.25	0.5	0.25	0.5	0.25	0.5
f_0 (MHz)	9.88	9.99	4.99	5.03	20.5	19.8

Table II.11: Resonators dimensions and mechanical resonance frequency values of each NEMS design.

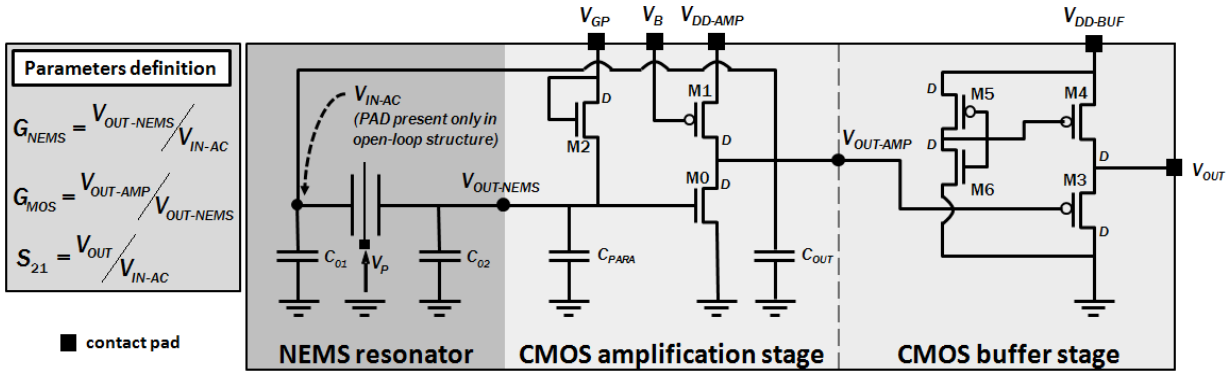


Figure II.3.3: Electrical schematic of the NEMS-CMOS self-oscillator and main parameters definition (on the left). D indicates the drain location of each transistor.

Transistors	M0	M1	M2	M3,6	M4	M5
W (µm)	1.2	6.7 (x10)	1	10	4	0.8
L (µm)	0.5	1	1	0.5	0.625	0.5

Table II.12: CMOS transistor dimensions.

III.3 Benchmarking

The current state-of-the-art features several demonstrators of M/NEMS-CMOS co-integrated oscillators, using various structural materials for the resonators (e.g. metal [Hua08-Ver11], mono- [Oll12] or polycrystalline silicon [Ver08-Zal10], silicon alloy [All09]) for various applications (pressure sensor [All09], time reference [Pac13-Che12], communication and data transfer [Hua08-Nab09], accelerometers [Tan11], gas and mass sensing [Ver11]). These devices rely on various CMOS technologies (AMS 0.35µm bulk CMOS [Ver08-Che12], CEA-LETI's FDSOI [Oll12], ON Semiconductor 1.5µm bulk CMOS [Zal10]). Two main oscillator architectures have been reported, namely Phase-Locked-Loop (PLL) and self-oscillating loop. The device fabricated here follows the latter approach with a monolithically integrated NEMS-CMOS self-oscillator using single-crystal Si resonator. Up to our knowledge, this oscillator constitutes the most compact NEMS-CMOS pixel (50x70µm²). A comparison with the state-of-the-art is provided in Table II.13 (the indicated devices areas include the NEMS resonator and the circuit without the contact pads).

References	Technology used	Resonator material/shape	Resonance frequency (MHz)	Device area (µm²)
[Nab09]	0.18µm	SiC / cantilever	8.29 and 11.59	6250000
[Li12]	TSMC 0.35µm	Metal / capacitive combs	0.117	298000
[Zal10]	ON S. 1.5µm	Si poly / dome	10-100	63000
[Ver08]	AMS 0.35µm	Metal / cantilever	6.32	60000
[Pac13]	TSMC 0.35µm	Metal / ring	1.39 and 9.34	37700
[Hua08]	TSMC 0.35µm	Nickel / disk	10.92	20600
This work	ST 0.35µm	Si mono / cantilevers	7-8	3500

Table II.13: State-of-the-art of NEMS-CMOS co-integrated oscillators. ON S. stands for ON Semiconductor.

III.4 NEMS-CMOS device characterization

An optimal solution consists in building a self-oscillating loop to develop a NEMS-based mass sensor. The suitable voltages that fulfill the Barkhausen conditions (see section III.4.3) must be determined. The open-loop characterizations of these devices are thereby primordial. It also enables an understanding and an estimation of the parasitic elements which can alter the operation of the device.

III.4.1 – CMOS circuit design and work analysis

As said before, the circuit is outstandingly compact since it contains only seven transistors (see Figure II.3.3) divided into two blocks. The amplification stage is composed by three transistors (from M_0 to M_2) and the buffer stage contains four transistors (from M_3 to M_6).

The goal of the transistor M_0 consists in amplifying the signal $V_{OUT\text{-}NEMS}$ from the resonators. This transistor is supplied in current by M_1 biased by V_B and $V_{DD\text{-}AMP}$ respectively applied on its gate and drain. M_1 is put in saturation regime and can be considered as a load resistance.

However, since the NEMS signal has no dc component, a voltage supply is necessary to polarize the gate of M_0. The transistor M_2 configured in active charge is used for this purpose and is monitored by a voltage V_{GP} acting both on its drain and

gate. M_2 acts as a polarization resistance R_{POL} which depends on the transconductance $g_{m\text{-}M2}$ and conductance $g_{ds\text{-}M2}$ of M_2 (II.96).

$$R_{POL} \approx \frac{1}{g_{m-M_2} + g_{ds-M_2}} [\Omega] \tag{II.96}$$

The other transistors constitute the unity gain buffer part. This buffer provides a necessary impedance matching since large capacitances due to bonding wires; pads and cables are present at the circuit output. These capacitances are around 10-20pF which may drastically affect the signal transmission as studied in the section I. More details about the guidelines of the circuit design are available in [Arn11b].

A small-signal modelling schematic of the NEMS resonator with the CMOS amplifier in open-loop configuration is shown in Figure II.3.4. C_{IN} corresponds to the total capacitance between the mechanical resonator and the gate of transistor M_0, such that:

$$C_{IN} = C_{02} + C_{PARA} + C_{GS-M_0} [\text{F}] \tag{II.97}$$

To avoid NEMS current losses through M_2, its dimensionsmust be chosen in order to maximize its impedance with respect to the overall capacitance C_{IN}, *i.e.*:

$$R_{POL} >> \frac{1}{C_{IN}\omega_{res}} [\text{F}] \tag{II.98}$$

By using the Millmann theorem, (II.99) can be obtained and simplified in (II.101) by designing properly M_0 and M_1according to (II.100). $H_{AMP\text{-}MOS}$ is the CMOS amplifier transfer function near the resonance frequency.

$$V_{OUT-AMP}(\omega_{res}) = \frac{(jC_{GD-M_0}\omega - g_{m-M_0})\cdot V_{OUT-NEMS}}{j(C_{GD-M_0} + C_{OUT})\omega + g_{ds-M_0} + g_{ds-M_1}} \approx -\frac{g_{m-M_0}}{jC_{OUT}\omega_{res}} \cdot V_{OUT-NEMS} [\text{V}] \tag{II.99}$$

$$C_{GD-M_0}\omega_{res} << g_{m-M_0} \quad ; C_{GD-M_0} << C_{OUT} ; \quad \frac{g_{ds-M_0} + g_{ds-M_1}}{C_{OUT}\omega_{res}} << 1 \tag{II.100}$$

$$H_{AMP-MOS} = \frac{V_{OUT-AMP}}{V_{OUT-NEMS}}(\omega_{res}) \approx -\frac{g_{m-M_0}}{jC_{OUT}\omega_{res}} \approx j\frac{g_{m-M_0}}{C_{OUT}\omega_{res}} \tag{II.101}$$

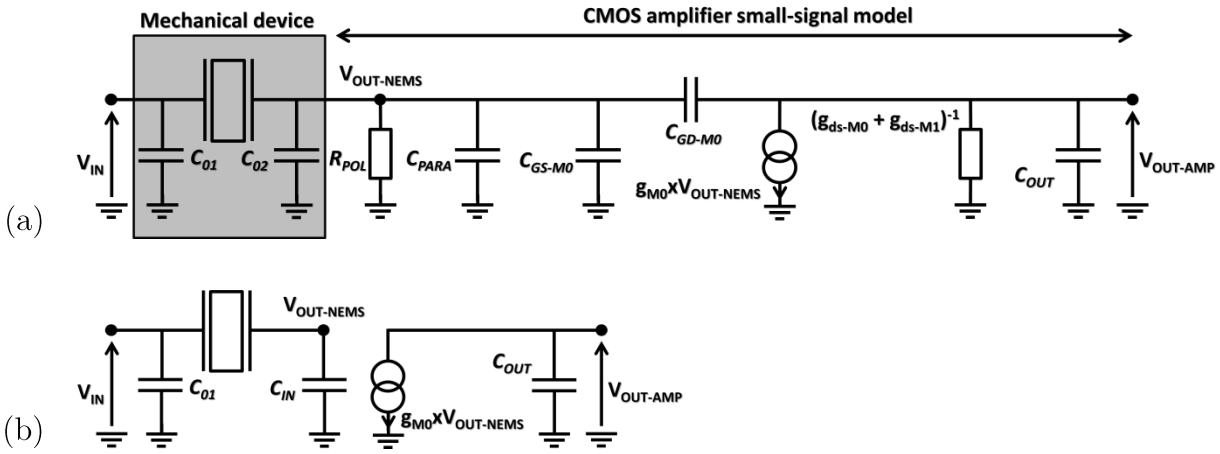


Figure II.3.4: Small-signal model of NEMS and CMOS amplifier before (a) and after (b) design considerations.

Consequently, the gain and phase-shift of the CMOS amplifier at resonance are respectively:

$$G_{AMP-MOS}(\omega_{res}) = \frac{g_{m-M_0}}{C_{OUT}\omega_{res}} \qquad \text{and} \qquad \varphi_{AMP-MOS}(\omega_{res}) = 90° \qquad \text{(II.102)}$$

As the NEMS resonator phase-shift is equal to -90° (II.79), the output capacitance C_{OUT} is necessary to fulfill the Barkhausen criteria and to have a zero total phase-shift (see section III.4.3).

III.4.2 – Open-loop characterization

In the frame of this thesis, the experimental characterization was performed in a vacuum chamber as illustrated in Figure II.3.5, with a network analyzer calibrated according to the cabling. The pressure inside the chamber was fixed at 0.05mbar.

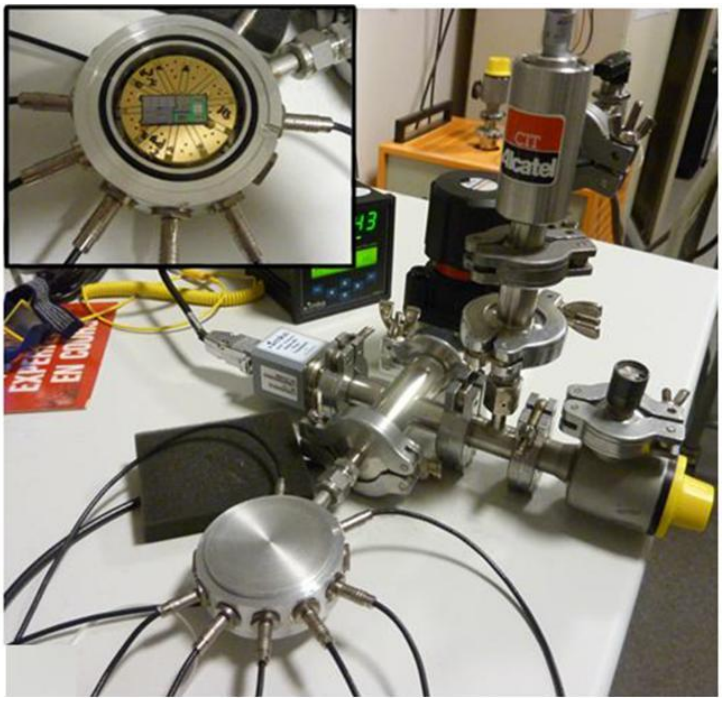


Figure II.3.5: Vacuum chamber bench used to characterize the selected devices, wire-bonded on a PCB. In the inset are depicted the chip and the PCB placed in the chamber.

III.4.2.1: CMOS circuit

The transfer function of the CMOS buffer $H_{BUF\text{-}MOS}$ and of the overall CMOS circuit $H_{MOS}$are given by (II.103) and (II.104) where G_{MOS} and φ_{MOS} correspond to its gain and phase-shift.

$$H_{BUF-MOS}(\omega)=\frac{V_{OUT}}{V_{OUT-AMP}}(\omega) \tag{II.103}$$

$$H_{MOS}(\omega)=H_{AMP-MOS}(\omega)\cdot H_{BUF-MOS}(\omega)=\frac{V_{OUT}}{V_{OUT-NEMS}}(\omega)=G_{MOS}e^{j\varphi_{MOS}} \tag{II.104}$$

The CMOS buffer is designed to work with a 3.3V supply voltage $V_{DD\text{-}BUF}$. Its frequency response is illustrated in Figure II.3.6 with an input power from the network analyzer fixed at -20dBm (~124mV peak-peak). This graph shows that its gain is lightly less than 0dB at low frequency (~1MHz).

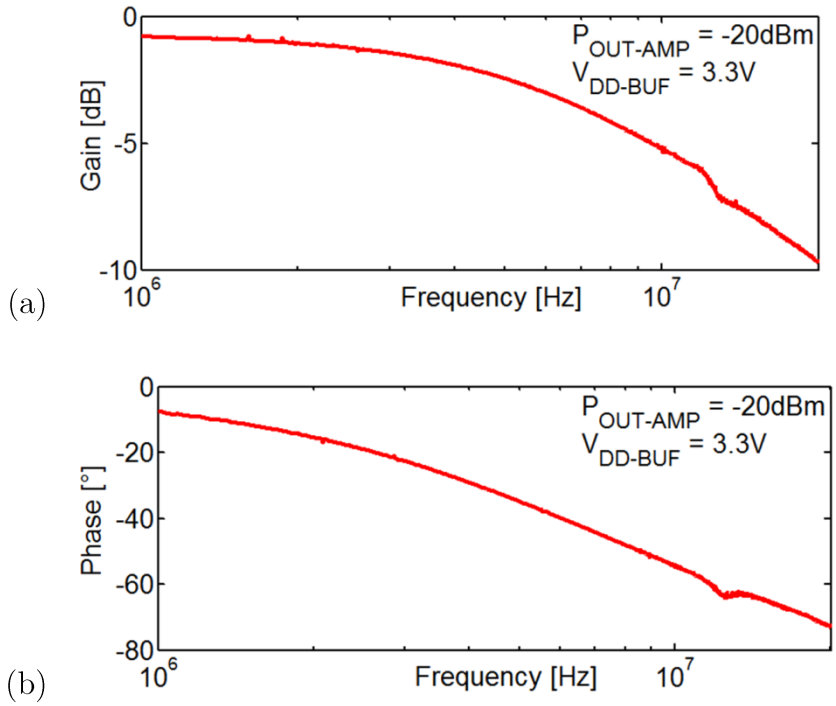


Figure II.3.6: Bode diagram with the gain (a) and phase-shift (b) frequency response of the CMOS buffer.

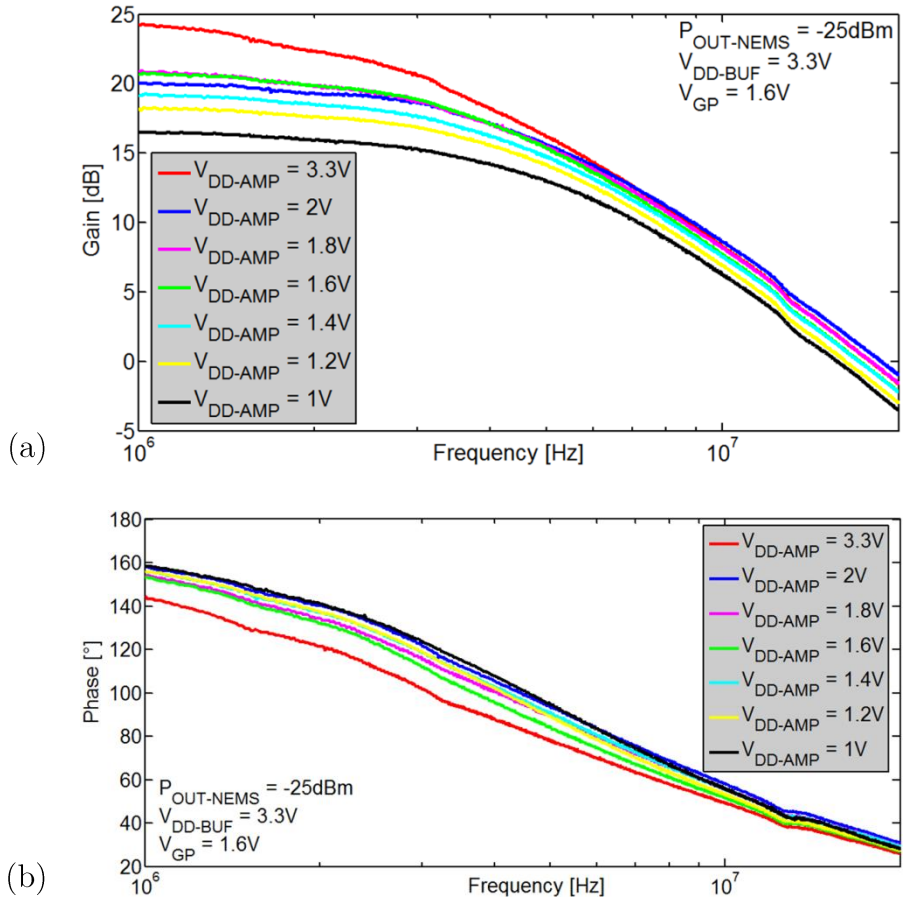


Figure II.3.7: Bode diagram with the gain (a) and phase-shift (b) frequency response of the overall CMOS circuit.

Figure II.3.7 corresponds to the Bode diagram of the complete circuit. The input power applied by the network analyzer is equal to -25dBm (72mV peak-peak). This graph shows that the gain decreases with the supply voltage $V_{DD\text{-}AMP}$. This may have an impact on the self-oscillating condition and particularly on the voltage V_P to apply on the cantilever. Table II.14 sums up the voltages and current consumptions with respect to the supply voltage $V_{DD\text{-}AMP}$ measured by sourcemeters.

$\mathbf{V_{DD\text{-}AMP}}$ **(V)**	1	1.2	1.4	1.6	1.8	2	3.3
$\mathbf{V_{GP}}$ **(V)**	1.6	1.6	1.6	1.6	1.6	1.6	1.6
$\mathbf{V_{B}}$ **(V)**	0.165	0.365	0.565	0.765	0.965	1.160	2.425
$\mathbf{I_{DD\text{-}AMP}}$ **(µA)**	71	74	74	74	75	77	96
$\mathbf{I_{DD\text{-}BUF}}$ **(mA)**	0.40	0.38	0.38	0.38	0.37	0.33	0.30

Table II.14: CMOS circuit operating points and current consumption evolution with respect to thesupply voltage $V_{DD\text{-}AMP}$ of the CMOS amplifier ($V_{DD\text{-}BUF} = 3.3$V).

III.4.2.2: NEMS-CMOS characterization

In order to experimentally demonstrate the electrical benefits of NEMS-CMOS integration, the frequency responses of two resonators with same dimensions were compared. One device was co-integrated with the CMOS circuit, and the other one was in a stand-alone configuration (*i.e.* without juxtaposed circuit). Both of them were from the same die (*i.e.* with identical process flow) and were driven with identical V_P and similar V_{IN} imposed by the network analyzer. Figure II.3.8 shows an outstanding 63dB signal improvement on resonance on the co-integrated resonator with respect to the stand-alone one. The resonance frequency can be identified and is close to 8.6MHz. A supply voltage $V_{DD\text{-}AMP}$ of 2V was used for the co-integrated device, thus according to Figure II.3.7, the CMOS circuit gain is almost 10dB at this frequency.

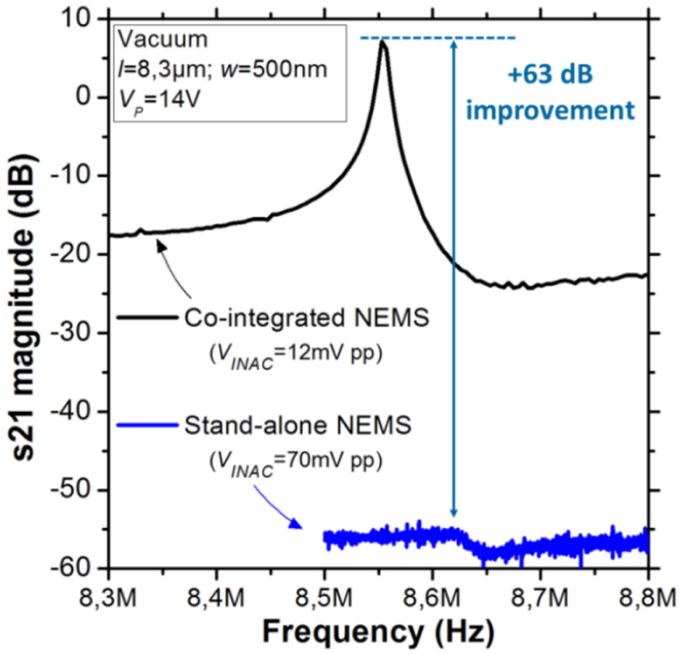


Figure II.3.8: Comparison of the frequency response in vacuum of two identical resonators driven with the same operating points, one being stand-alone and the other co-integrated (s21 is defined in Figure II.3.3). A supply voltage $V_{DD\text{-}AMP}$ of 2V was applied in the co-integrated system [Arc12].

The extra 53dB enhancement is related to the difference of about three orders of magnitude in the NEMS output capacitance, which will be demonstrated in the subsequent section. In this sense, although having a low gain, the circuit efficiently interfaces the NEMS resonator with the outside world, its main role being to compensate the impedance mismatches. Noteworthy is the nosiest signal of the stand-alone device (in spite of a six times larger actuation force), what illustrates the SNR improvement provided by CMOS integration. The immunity to parasitics and feedthrough is also clearly better as the SBR is largely improved (almost 30dB against few dB), presumably because the CMOS-amplified NEMS output signal is much larger than the feedthrough signal.

The frequency response of different NEMS devices was studied with an input power P_{IN} of -35dBm (*i.e.*22mV peak-peak) and for different cantilever voltages V_P, whereas the CMOS amplifier and buffer (*i.e.* $V_{DD\text{-}BUF}$ and $V_{DD\text{-}AMP}$) were supplied with a 3.3V voltage. The other CMOS voltages were selected according to Table II.13. Figure II.3.9 depicts the performances of a NEMS-CMOS system using a PEL1P design (cf. Table II.10) for various V_P. Compared to the theoretical case (Figure II.2.6 and II.2.7), a larger phase-shift can be observed for high V_P voltages. The contribution of the feedthrough effect and the CMOS phase response are responsible of this additional phase-shift present after the resonance.

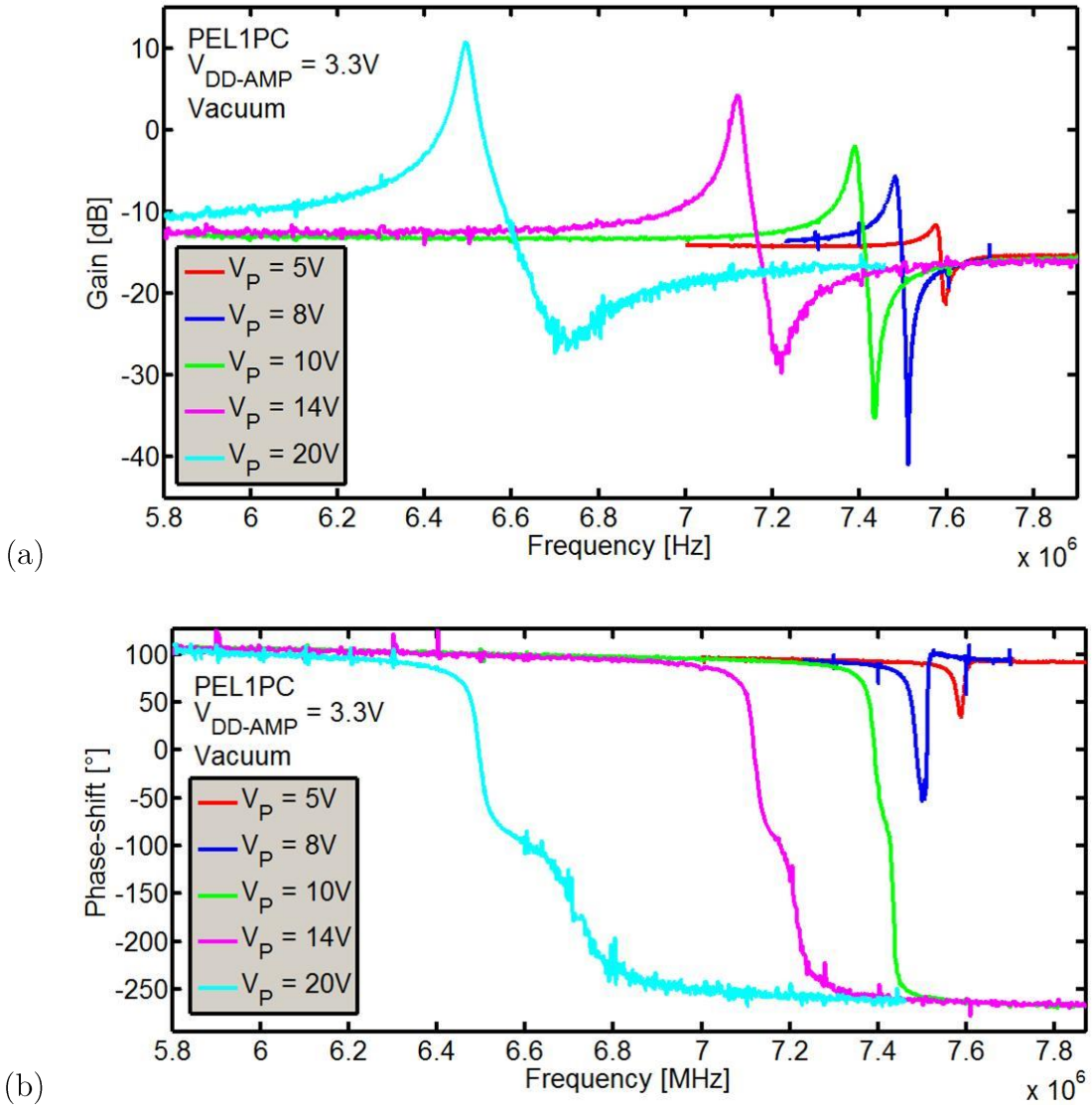


Figure II.3.9: Bode diagram with gain (a) and phase-shift (b) frequency response of a NEMS-CMOS system using a PEL1P structure.

III.4.2.3: Parameters extraction and analysis

All these frequency responses were modelled using expressions (II.105) and (II.106) in order to extract the resonator parameters, *i.e.* f_{res}, Q, and G_{NEMS} for each V_P. For the fit, the feedthrough transfer function is expressed by a complex number with $H_{ft\text{-}real}$ and $H_{ft\text{-}imag}$ respectively as real and imaginary parts. Moreover, an additional phase-shift ψ comprising the CMOS circuit one and the apparatus measurement one is considered in the model.

$$H_{res}(f)=\left(\frac{G_{NEMS}}{1-\left(\frac{f}{f_{res}}\right)^2+j\frac{f}{f_{res}Q}}+H_{ft-real}+jH_{ft-imag}\right)G_{MOS}e^{j\Psi} \quad \text{(II.105)}$$

with $$G_{NEMS}=\frac{\varepsilon_0^2 e^2 a^2 V_{dc}\left(V_{dc}-V_{out-dc}\right)}{g^4 k C_{IN}} \quad \text{(II.106)}$$

V_{dc} and $V_{out\text{-}dc}$ respectively correspond to V_P and V_{GP} according to Figure II.3.3.

Fits of experimental results are illustrated on Figures II.3.10 and II.3.11 for a NEMS-CMOS structure using PEL1P design. These graphs show a good agreement between the experimental results and the theoretical model. Extracted parameters values for these particular cantilever voltages are given in Table II.15.

V_P (V)	f_{res} (MHz)	Q	G_{NEMS}	$H_{ft\text{-}real}$	$H_{ft\text{-}imag}$	G_{MOS}	Ψ(°)
5	7.58	388	$5.62\text{x}10^{-5}$	$2.27\text{x}10^{-2}$	$4.46\text{x}10^{-3}$	7.94	-98.5
8	7.49	372	$1.70\text{x}10^{-4}$	$2.25\text{x}10^{-2}$	$5.62\text{x}10^{-3}$	8.03	-100
10	7.39	361	$2.80\text{x}10^{-4}$	$2.20\text{x}10^{-2}$	$5.80\text{x}10^{-3}$	8.22	-100
12	7.27	340	$4.27\text{x}10^{-4}$	$2.24\text{x}10^{-2}$	$3.88\text{x}10^{-3}$	8.41	-94.0
14	7.12	315	$6.22\text{x}10^{-4}$	$2.26\text{x}10^{-2}$	$2.55\text{x}10^{-3}$	8.61	-88.4
16	6.94	279	$8.44\text{x}10^{-4}$	$2.17\text{x}10^{-2}$	$5.35\text{x}10^{-3}$	9.02	-95.2
18	6.73	267	$1.44\text{x}10^{-3}$	$2.08\text{x}10^{-2}$	$5.27\text{x}10^{-3}$	9.33	-94.7
20	6.49	241	$1.50\text{x}10^{-3}$	$2.08\text{x}10^{-2}$	$5.63\text{x}10^{-3}$	9.77	-91.9

Table II.15: Parameter values extracted from the fit of the experimental results for different V_P.

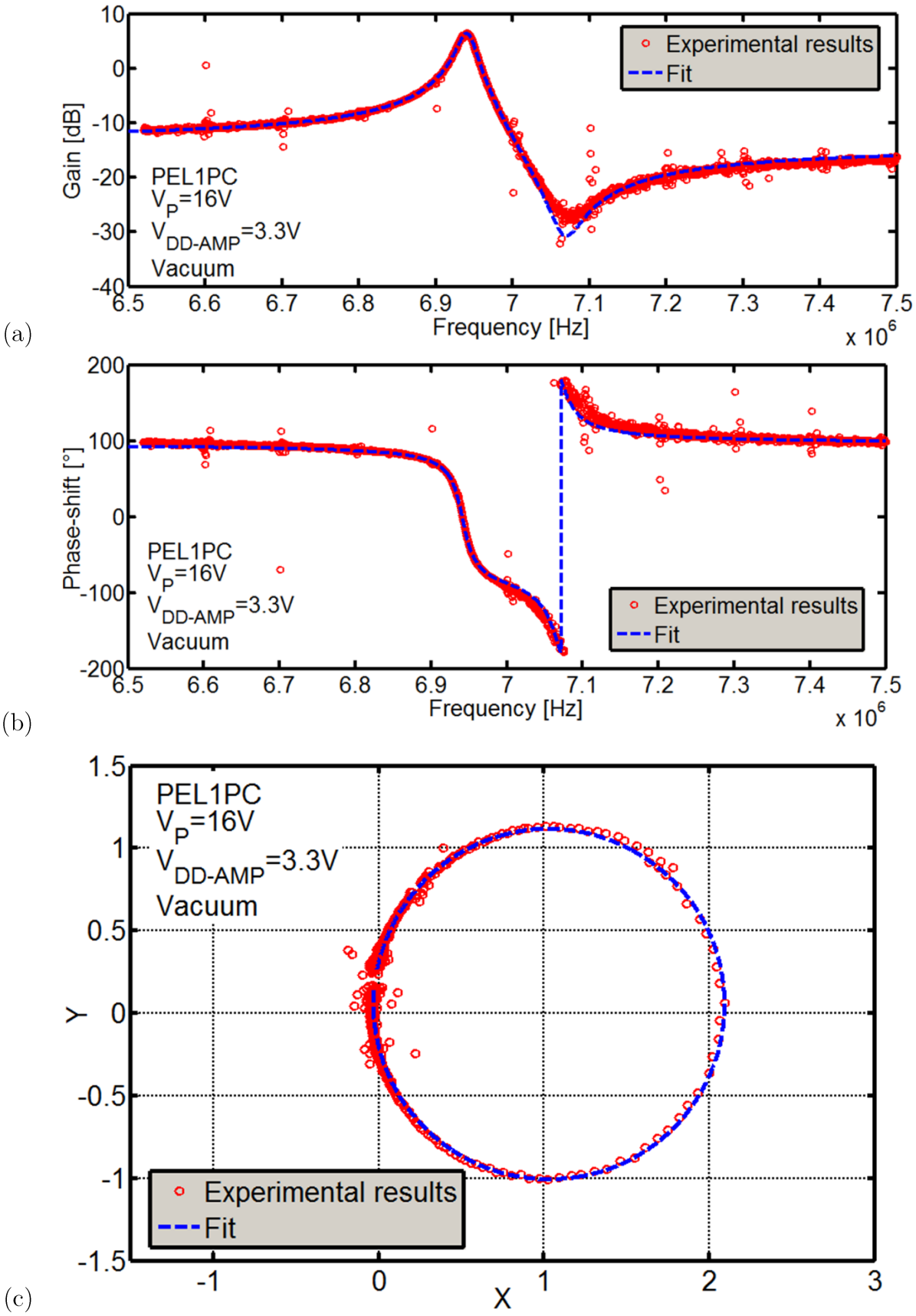


Figure II.3.10: Experimental results and fits of gain (a), phase-shit (b), X and Y (c) evolution versus frequency for V_P=16V.

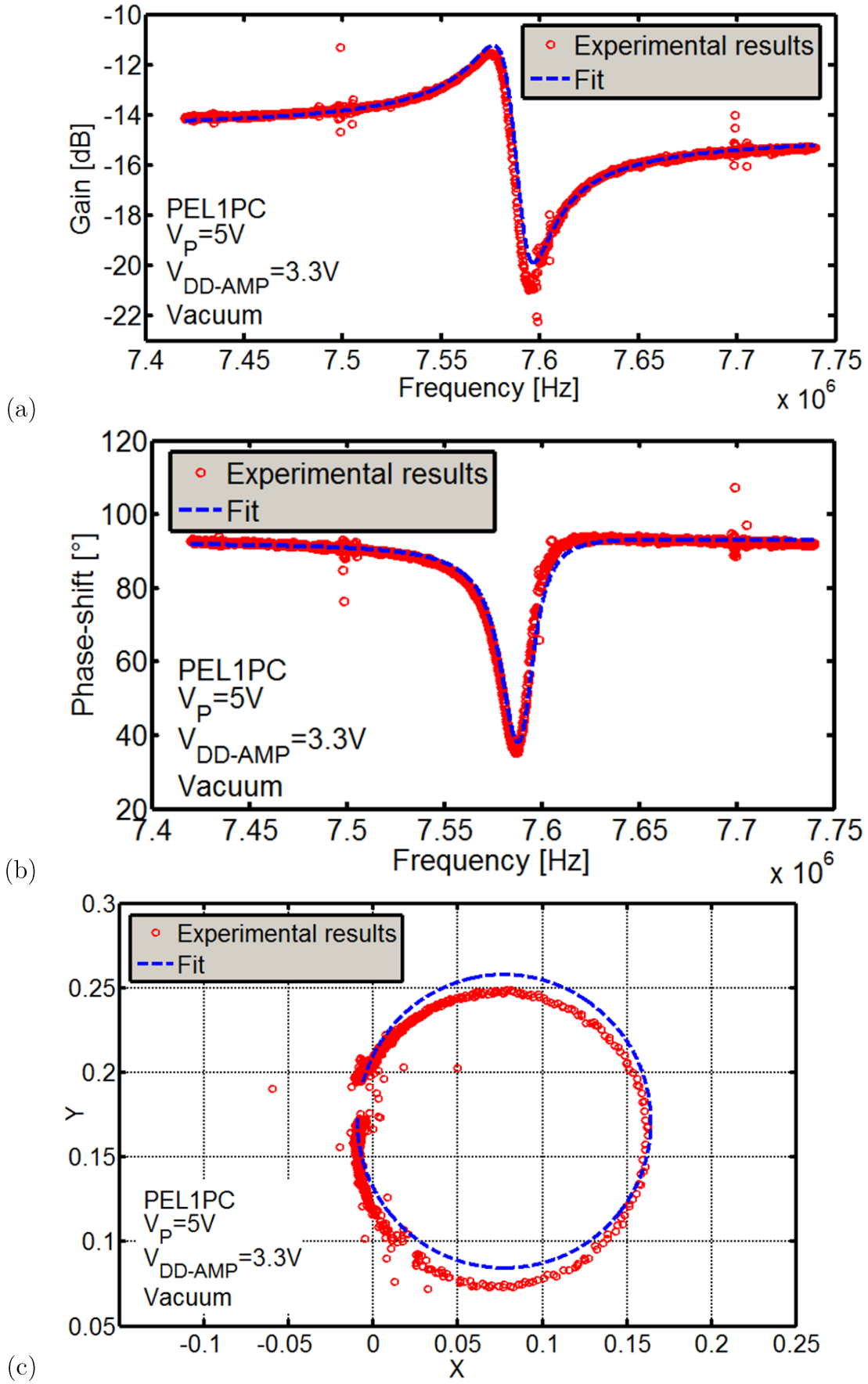


Figure II.3.11: Experimental results and fits of gain (a), phase-shit (b), X and Y (c) evolution versus frequency for a V_P=5V.

Figure II.3.9 and parameters extraction show:

- a resonance and anti-resonance peak due to a feedthrough signal can be observed;
- the resonance frequency and the quality factor decrease while the gain at resonance increases when the cantilever voltage V_P rises.

Because of the electrostatic forces applied on the beam (as represented in Figure II.3.12), the stiffness coefficient k_{eff} varies with V_P, which alters the resonance frequency f_{res}. This phenomenon, so-called spring-softening effect, may be analyzed using equation (II.33) expressed below (II.107) where k_0 is the stiffness coefficient of the structure without any forces applied on the cantilever, F_1 and F_2 are respectively the electrostatic forces of the system {actuation electrode / beam} and {transduction electrode / beam}:

$$m\ddot{y} + c\dot{y} + k_0 y = F_1 - F_2 \tag{II.107}$$

$$\text{with} \quad F_1 = \frac{\varepsilon_0 ea\left(V_p - V_{in-AC}\right)^2}{2(g-y)^2} \qquad \text{and} \qquad F_2 = \frac{\varepsilon_0 ea\left(V_p - V_{out-NEMS}\right)^2}{2(g+y)^2} \tag{II.108}$$

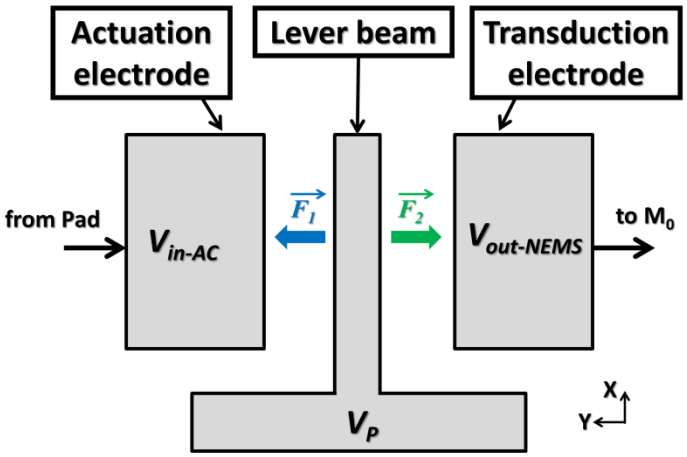


Figure II.3.11: Schematic of the NEMS resonator under electrostatic forces F_1 and F_2.

Since $V_{in-AC} << V_P$ as presented in section II.1 and $y << g$, a Taylor expansion can be used until the first order to obtain:

$$m\ddot{y} + c\dot{y} + k_0 y \approx \frac{\varepsilon_0 ea}{2g^2}\left[V_{out-NEMS}\left(2V_P - V_{out-NEMS}\right)\right] + \frac{\varepsilon_0 ea}{2g^2}\cdot\frac{2y}{g}\left[V_P^2 + \left(V_P - V_{out-NEMS}\right)^2\right] \tag{II.109}$$

According to Figure II.3.3, $V_{out\text{-}NEMS}$ corresponds to V_{GP}, leading to:

$$m\ddot{y} + c\dot{y} + \underbrace{\left(k_0 - \frac{\varepsilon_0 ea}{g^3}\left[V_P^2 + (V_P - V_{GP})^2\right]\right)}_{k} y \approx \underbrace{\frac{\varepsilon_0 ea}{2g^2}\left[V_{GP}(2V_P - V_{GP})\right]}_{F_{elec}} \qquad \text{(II.110)}$$

From (II.110), two terms emerge: k represents the stiffness coefficient including the spring-softening effect and F_{elec} is the resulting electrostatic force acting on the beam. Consequently, an increase of V_P makes decreasing the stiffness coefficient and also the resonance frequency. This spring-softening effect is experimentally verified on each structure. Figure II.3.13 depicts the resonance frequency evolution on PEL1P structure.

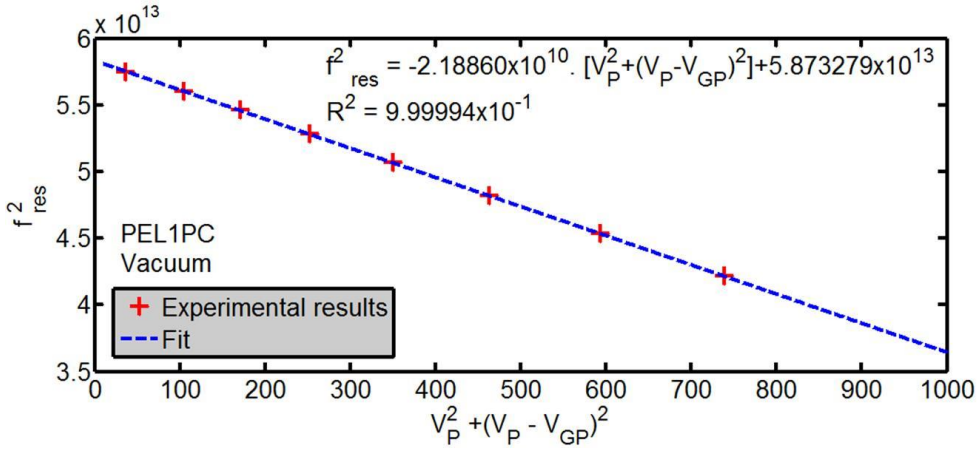


Figure II.3.13: Resonance frequency evolution of the PEL1P structure with the cantilever and CMOS amplifier M_0 gate voltages. R corresponds to the correlation coefficient between the fit and the experimental results.

The intercept of the fit corresponds to the square value of the mechanical resonance frequency. This frequency around 7.6MHz is far from the one expected, *i.e.* 9.9MHz. This can be explained by the device dimensions slightly different from the original design due to some lithography uncertainties. The new dimensions were measured through SEM micrographs and are given in Table II.16. After the determination of mass m_{eff} taking into account these new dimensions, k can therefore be determined with respect to V_P. Figure II.3.14 depicts a slight variation of k. As a consequence, this coefficient can be consideredas constantwithin the V_P range.

Device	L (µm)	w (nm)	e (µm)	g (nm)	a (µm)	m (fg)	f_0(MHz)
Original	5.90	250	1.00	250	5.40	2.20	9.9
Measured	6.33	220	1.00	310	5.80	2.07	7.6

Table II.16: Dimensions comparison of a PEL1P resonator structure.

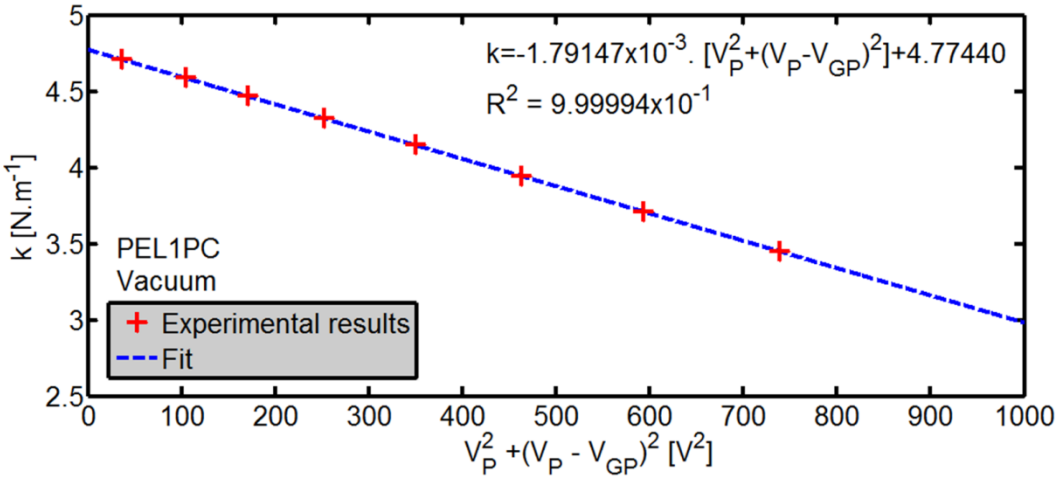


Figure II.3.14: Stiffness variation of the PEL1P structure with the cantilever and CMOS amplifier M_0 gate voltages.

The model describing the NEMS gain G_{NEMS} expressed in (II.106) is compared to the experimental results. It appears that it correctly fits the experimental results, as presented in Figure II.3.15.

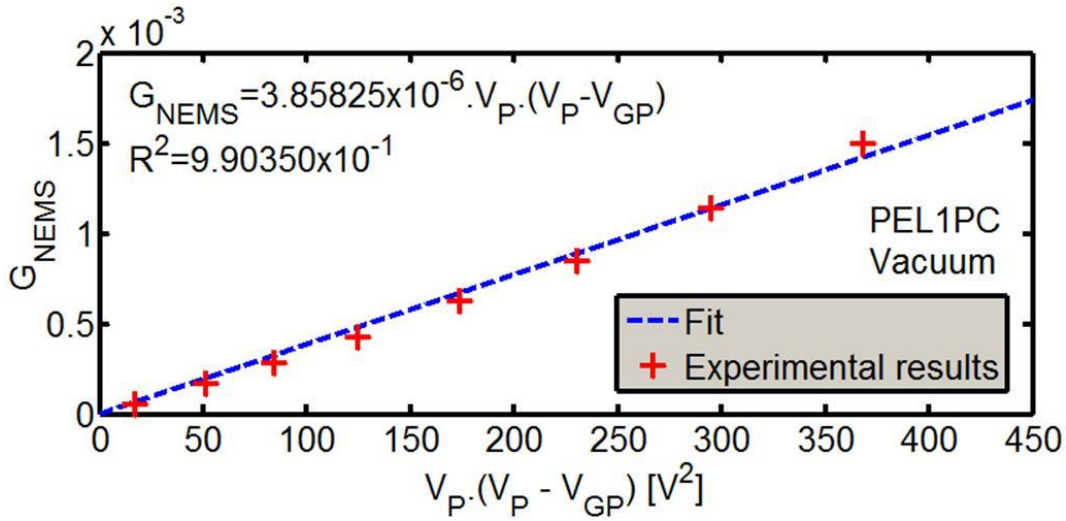


Figure II.3.15: NEMS gain variation of the PEL1P structure with the cantilever and CMOS amplifier M_0 gate voltages.

The quality factor variation is also investigated. Figure II.3.16 depicts a decrease of Q when V_P increases. This behavior is explained by the spring-softening effect since quality factor Q and stiffnesscoefficient $k$are linked through equation (II.111).

$$Q = \frac{\sqrt{km}}{c} \tag{II.111}$$

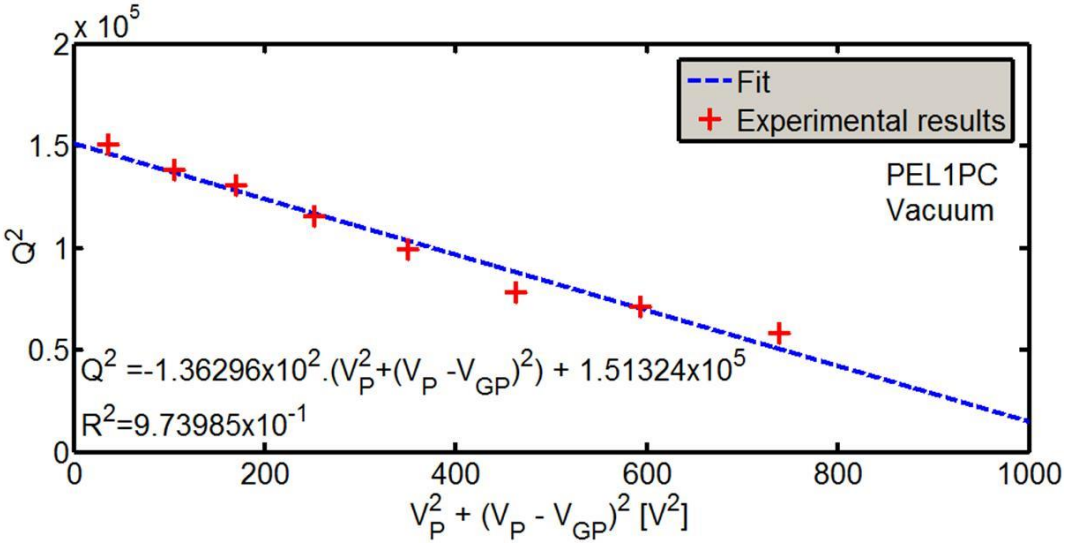


Figure II.3.16: Quality factor variation of the PEL1P structure with the cantilever and CMOS amplifier M_0 gate voltages.

This modelling makes possible the determination of the input capacitance C_{IN} between the NEMS and the CMOS circuit. Indeed, the development of (II.106) gives:

$$V_P(V_P - V_{GP}) = C_{IN}.\frac{G_{NEMS}.Y.f_{res}^2}{Q} \quad \text{with} \quad Y = \frac{4\pi^2 g^2 m}{C_0^2} \text{ and } \quad C_0 = \frac{\varepsilon_0 ea}{g} \tag{II.112}$$

According to (II.97), C_{IN} is composed by C_0, $C_{GS\text{-}M0}$ and C_{PARA} respectively the NEMS, M_0 gate-source and interconnect capacitance. The latter was calculated using a co-integrated and a stand-alone device, as described in Figure II.3.17. This overall capacitance is evaluated around 19.8fF and 5.70pF respectively for co-integrated and stand-alone configuration. Furthermore, $C_0$and $C_{GS\text{-}M0}$ are around 0.165fF and 0.201fF. These values were determined from the SEM micrographs and electrical measurements of M_0 transistor. These two values have a poor impact on C_{IN} which mostly depends on the interconnection capacitance C_{PARA}. Both of these values correctly match with the expected one described in the first section of this chapter.

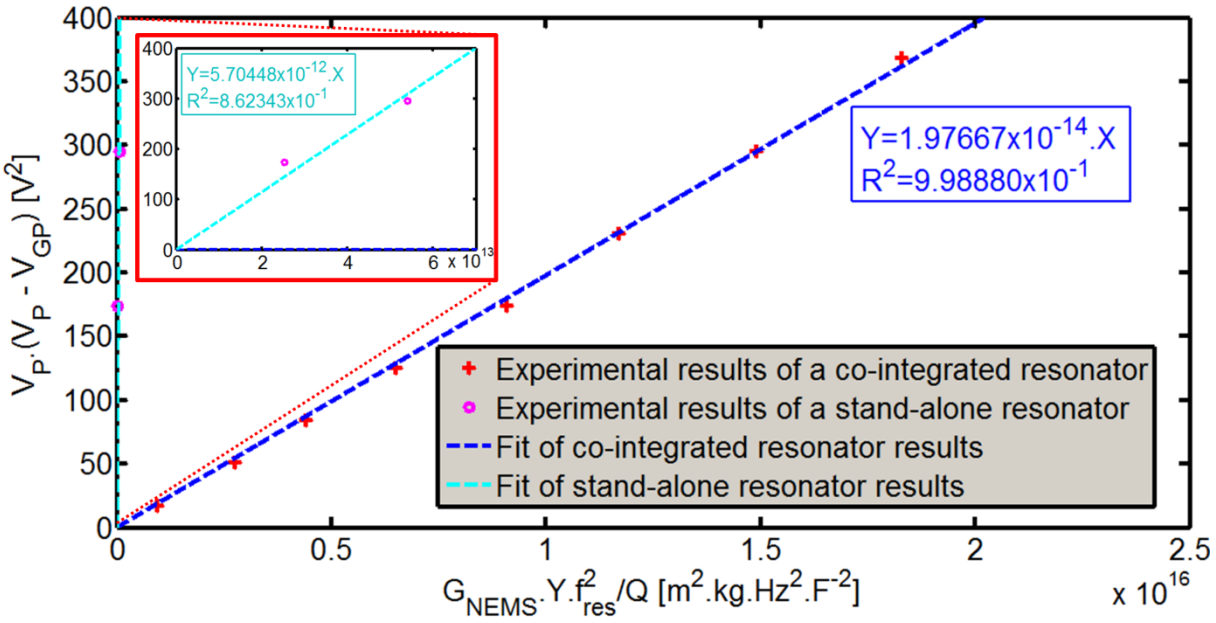


Figure II.3.17: Parasitic capacitance C_{PARA} determination for stand-alone (in light blue) and co-integrated (in dark blue) device.

Another important parameter concerns the feedthrough transfer function. Table II.14 shows the predominance of $H_{ft\text{-}real}$ with respect to $H_{ft\text{-}imag}$. Moreover, this coefficient does not change with the frequency as observed in the Bode diagrams of Figure II.3.10 and II.3.11. Modelling this parasitic parameter as a capacitance C_{ft} is thereby relevant in a first approximation. This capacitance may come from the fringing field effect between actuation and detection ports.

The sensitivity at the resonance frequency (defined in II.3) was also investigated. Figure II.3.18 depicts the normalized sensitivity $S_{MAX\text{-}red}$ variation measured with respect to the H_{ft}/G_{NEMS} ratio for a PEL5P structure. These experimental data were compared to the semi-empirical model expressed in (II.89) (in blue) and to the ideal model (*i.e.* without parasitic feedthrough effect) expressed in (II.82) (in green) using the parameters extracted from the open-loop characterizations. Equation (II.89) seems to correctly describe the experimental behavior. Moreover, it appears that feedthrough effects do not have a strong influence on the maximum sensitivity if it does not exceed one hundred times the value of the resonator gain G_{NEMS}, as theoretically observed in section II (see Figure II.2.8).

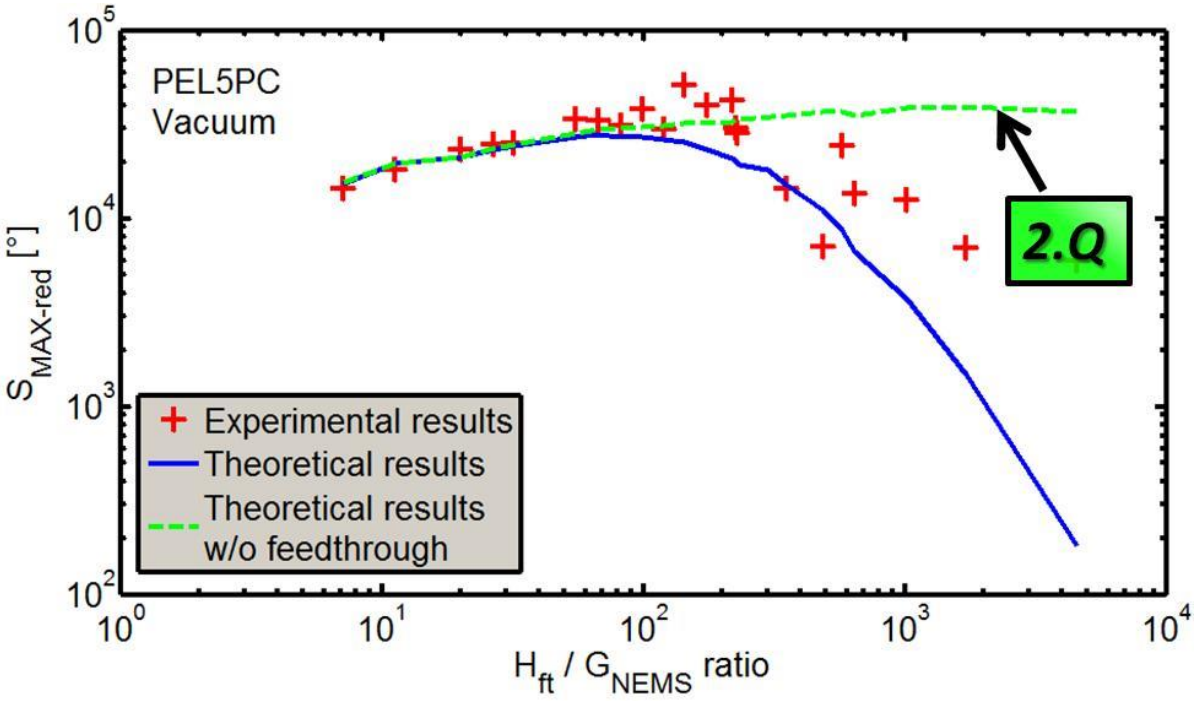


Figure II.3.18: Experimental results of sensitivity measured at the resonance frequency (in red) compared with the ideal (in green) and the real (in blue) semi empirical model.

III.4.3 – Closed-loop characterization and demonstration of self-oscillator

This part will focus on the implementation of a self-oscillating loop. For this purpose, the NEMS-CMOS open-loop transfer function $H_{OL}(f)$ must respect the Barkhausen criteria

$$H_{OL}(f) = H_{elec}(f) \cdot H_{res}(f) \tag{II.113}$$

where $H_{elec}(f)$ and $H_{res}(f)$ are the transfer function of the electronic feedback circuit and of the NEMS device. Self-oscillations appear at a frequency f_{osc} only if those two criteria are fulfilled, *i.e.*:

$$\left|H_{OL}(f_{osc})\right| \geq 1 \qquad \text{and} \qquad \arg\left[H_{OL}(f_{osc})\right] = 0° \tag{II.114}$$

(II.114) is equivalent to:

$$\begin{cases} G_{res}(f_{osc}) \cdot G_{elec}(f_{osc}) \geq 1 \\ \varphi_{res}(f_{osc}) + \varphi_{elec}(f_{osc}) = 0° \end{cases} \tag{II.115}$$

As a consequence, the electronic circuit has to be designed and supplied carefully according to the resonator parameters in order to set the system into oscillation.

III.4.3.1: Barkhausen conditions fufillment

Open-loop characterizations of the system are first necessary in order to retrieve the suitable NEMS polarizations (V_P) and electronic circuit voltages (V_{GP}, V_B, $V_{DD\text{-}AMP}$, $V_{DD\text{-}BUF}$) that fulfill the Barkhausen conditions expressed in (II.115). Both gain and phase shift are determined for several supply voltages $V_{DD\text{-}AMP}$ of the amplification stage and for several beam polarizations V_P. V_{GP} and V_B are adjusted according to $V_{DD\text{-}AMP}$ (see Table II.13) in order to get a maximal gain of the CMOS amplifier. According to the design of the buffer stage, $V_{DD\text{-}BUF}$ is fixed at 3.3V for a better impedance matching with external measurement apparatus. An example of frequency response is shown on Figure II.3.19, which is obtained for $V_{DD\text{-}AMP}$ 3.3V. As the output of the CMOS amplification stage is directly linked to the NEMS input in closed-loop configuration (see Figure II.3.3), the buffer contribution must be suppressed in order to retrieve the contribution of the NEMS and the CMOS amplifier.

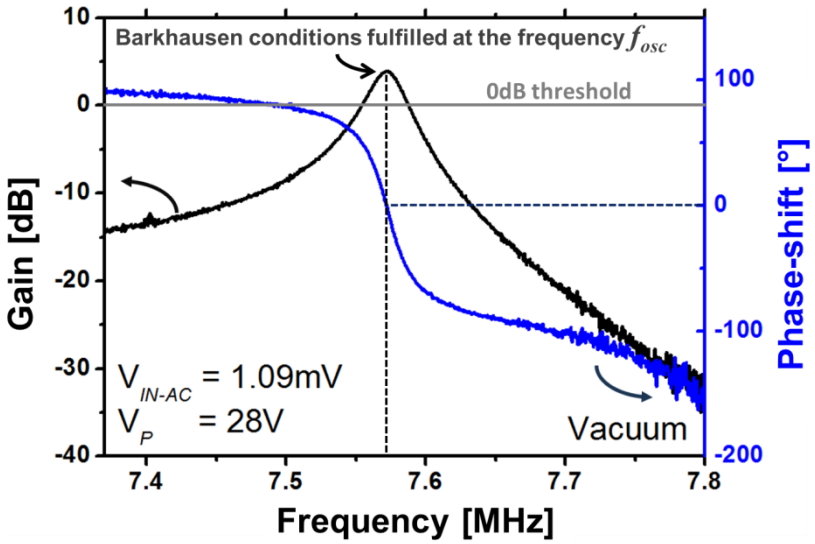


Figure II.3.19: Electrical open-loop response in vacuum of the NEMS CMOS system. The Barkhausen criteria are satisfied at the frequency f_{osc}.

III.4.3.2: Steady-state of self-oscillations study

Thanks to the previous study, it is possible to determine the minimal NEMS voltage V_P fulfilling the Barkhausen conditions as a function of the CMOS amplifier supply voltage $V_{DD\text{-}AMP}$, and so the theoretical feasibility of the self-oscillator. However, these results are not sufficient to predict the stability of the device. Indeed a saturation mechanism is required to stabilize the oscillation amplitude at a value smaller that the pull-in distance. A possible solution consists in designing a limiter circuit. Nevertheless

this option is potentially area and power consuming. Thus, the CMOS amplification stage was designed such that the oscillation's amplitudes are limited by the saturation of the circuit. This method makes this system very simple and compact. Before the characterization of the structure in closed-loop configuration, an electrical study of the amplifier stage was performed in order to determine the gain variations for different ac input signals and supply voltages $V_{DD\text{-}AMP}$ at the oscillation frequency f_{osc}.

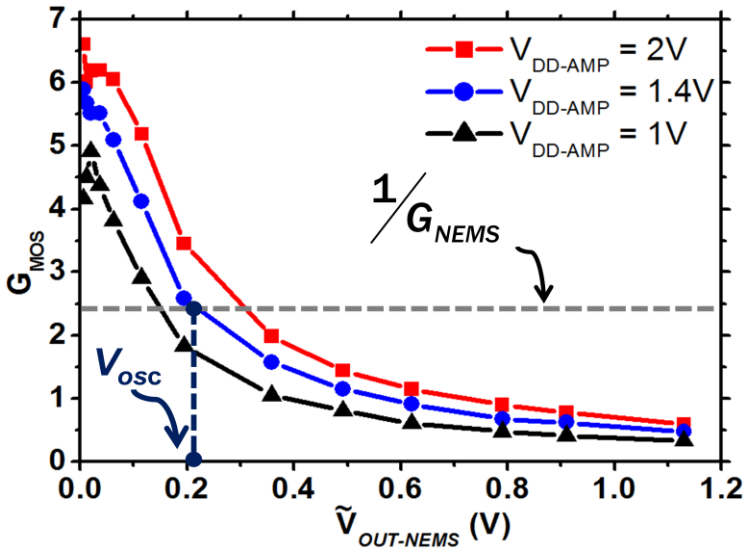


Figure II.3.20: CMOS amplifier response at the oscillation frequency f_{osc} as a function of the circuit ac input voltage $\tilde{v}_{OUT\text{-}NEMS}$ and for different circuit supply voltages. This graph allows extracting the maximum NEMS oscillation amplitude voltage V_{OSC} before pull-in collapse.

Figure II.3.20 depicts the CMOS amplifier response at f_{osc} with respect to the ac term of the NEMS output voltage $\tilde{v}_{OUT\text{-}NEMS}$ for different $V_{DD\text{-}AMP}$. This graph shows that the CMOS gain is increasing with $V_{DD\text{-}AMP}$ for a same $\tilde{v}_{OUT\text{-}NEMS}$. The latter is directly proportional to the mechanical amplitude X_{NEMS} of the beam according to (II.116).

$$X_{NEMS} = \frac{V_{OSC} \cdot C_{IN} \cdot g^2}{V_P \cdot \varepsilon_0 \cdot S} \tag{II.116}$$

In order to evaluate V_{OSC} and X_{NEMS}after generation of the self-oscillations, G_{MOS} and G_{NEMS} (extracted using the model described in (II.105)) are plotted on the same graph. The value of V_{OSC} is given by the intersection abscissa point of G_{MOS} and $1/G_{NEMS}$. In Figure II.3.20 is shown the case where V_{OSC} is determined for $V_{DD\text{-}AMP}$ equal to 1.4V. For the preservation of the system integrity during the steady-state oscillations, X_{NEMS} must not exceed a 50% of the gap g (as depicted in Figure II.3.21), which means that V_{OSC} must not be larger than a certain value. Furthermore, for a

same given value of $1/G_{NEMS}$, V_{OSC}(and so X_{NEMS}) is decreasing with $V_{DD\text{-}AMP}$. Figure II.3.21 shows an example for a given V_P voltage. The induced $1/G_{NEMS}$coefficient intercepts G_{MOS} for the three different $V_{DD\text{-}AMP}$. X_1 and X_2 respectively correspond to the abscissa of the intersection point for $V_{DD\text{-}AMP}$ at 1V and 2V. For the self-oscillator integrity, the best solution consists in supplying the CMOS amplifier at 1V, since the oscillations amplitude is below the half of the gap, which is not the case for a 2V (and also 1.4V) $V_{DD\text{-}AMP}$. In conclusion, the safest approach to generate self-oscillations is first to work with a low value of $V_{DD\text{-}AMP}$, and then finding the V_P threshold value fulfilling the Barkhausen criteria. The selection of this polarization is crucial for the amplitude oscillation limitation because of the dependence between G_{NEMS} and V_P explained in (II.106).

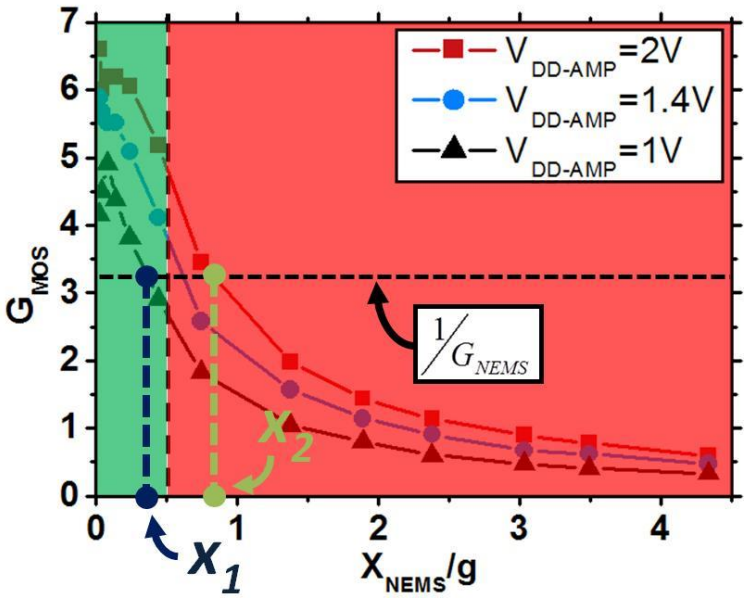


Figure II.3.21: CMOS amplifier response at the oscillation frequency f_{osc} as a function of the ratio of amplitude oscillation X_{NEMS} over g for different amplifier supply voltages and for a given V_P. The green and red zones respectively correspond to the zones below and beyond the safety oscillation amplitudes (50% of g).

III.4.3.3: Generation of self-oscillations in vacuum

Self-oscillations were obtained with 1.4V supply voltage $V_{DD\text{-}AMP}$ and a 24V cantilever voltage V_P. Figures II.3.22 and II.3.23 respectively depict the time-domain and frequency-domain steady-state electrical response of the NEMS-CMOS self-oscillator.

The self-oscillations are stabilized at 7.83MHz with a 0.18V rms amplitude, without any other parasitic oscillations over a wide spectrum. This result shows the strong interest of the co-integrated NEMS-CMOS strategy for oscillators' realization because better SNR and SBR are achieved and the monolithic connection between the electronic and the mechanical parts provides less parasitic oscillations with respect to the off-chip configuration.

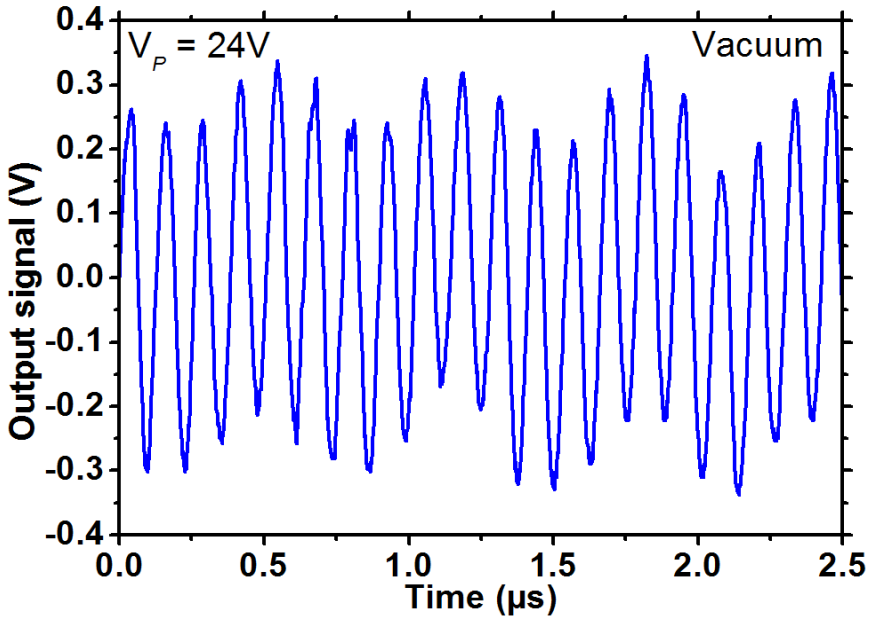


Figure II.3.22: Output (V_{OUT}) time-domain steady-state signal of the NEMS-CMOS closed-loop in vacuum (0.05mbar).

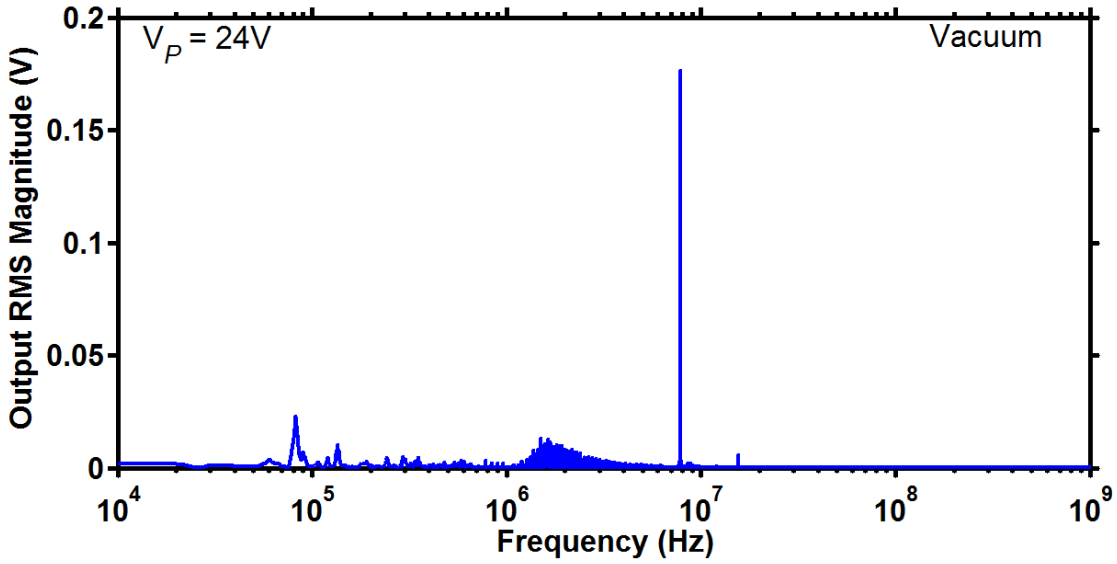


Figure II.3.23: Fast-Fourier transform of the closed-loop output signal (V_{OUT}): the NEMS-CMOS signal is the single peak of the spectrum (no parasitic oscillations). This electrical measurement was performed in vacuum (0.05mbar).

IV. Discussion and conclusion

In this chapter, a study of signal transmission for different kind of interconnects previously described in chapter I was proposed. It appears that monolithic integration constitutes a favorable solution since the electrical signal between NEMS and CMOS is not impacted.

Furthermore, a self-oscillator based on c-Si capacitive NEMS resonators co-integrated with a low cost and compact CMOS circuitry was demonstrated. A detailed study of the open-loop electrical response was first necessary to retrieve the Barkhausen conditions while ensuring the system would stabilize at an oscillation amplitude smaller than the pull-in distance. The use of the CMOS saturation constitutes a very simple way to limit the oscillations and to preserve the integrity of the mechanical part when compared to other solutions such as a limiter circuit. As a very compact and functional oscillator is achieved, this device paves the way for ultra-dense arrays of NEMS-CMOS oscillator pixels for emerging applications, such as gas sensors or mass spectrometers.

This device was fabricated following a 2D approach. This architecture can be further optimized to a target mass sensor based on a high density of NEMS resonators located above the CMOS circuit. Such integration scheme constitutes the object of the next chapter.

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Chapter III

Towards 3D monolithic co-integration between NEMS and CMOS

The previous chapter presented an experimental demonstration of a two-dimensional co-integration between NEMS and CMOS. This chapter proposes to investigate the feasibility of an original monolithic integration which consists in implementing monocrystalline silicon (c-Si) NEMS resonators above both the CMOS circuit and the back-end interconnections. In a first time, this section will provide definitions of the major microelectronic fabrication steps used for this NEMS-CMOS development. The process flow chosen for such a technology will be detailed and discussed afterwards regarding its advantages and issues with respect to other existing solutions. The final part will focus on three main technological modules which characterize this 3D monolithic above-IC integration.

I. 3D NEMS-CMOS presentation

In chapter I was demonstrated the capability of NEMS resonators as promising solution for mass detection application. In order to fabricate a real-time sensor, these electromechanical systems must be integrated with a CMOS circuit. An overview on different possible integration between NEMS and CMOS was also presented in this chapter. The best solution consists in following a monolithic approach, *i.e.* developing all the devices on the same die. This fact was proven in terms of electrical performance in chapter II which described an example of two dimensional (2D) co-integration. The following chapter will now focus on another kind of assembly using the three dimensions.

I.1 Problematic

One main asset of hybrid integration approaches is the possibility to develop a three dimensional (3D) M/NEMS-CMOS stack without impacting the fabrication of electronic or sensing part. Each stand-alone method has its own advantages and drawbacks. TSVs approach offers an attractive trade-off between area consumption, throughput (W2W integration possible) and direct contact between NEMS and environment (no encapsulation). However, such a scheme suffers not only from parasitic capacitance causing signal attenuation (see section I of chapter II), but also from a high pitch due to KOZ. The latter considerably affects the resonators density for array construction. Moreover, alignment accuracy during interconnect fabrication constitutes another issue. Figure III.1.1 shows that alignment performance is superior to 1µm if the interconnect width is above 1µm, which corresponds to the same size of TSVs (refer to Table I.2 in chapter I). Such behavior precludes the use of these vias and encourages creation of shorter interconnects improving thereby NEMS array density. Even if 3D interconnects (presented in section III.1.2 of chapter I) provide tiny contact width, most of them requires thermo-compression process, many fabrication steps and have a low throughput (only D2D or D2W possible).

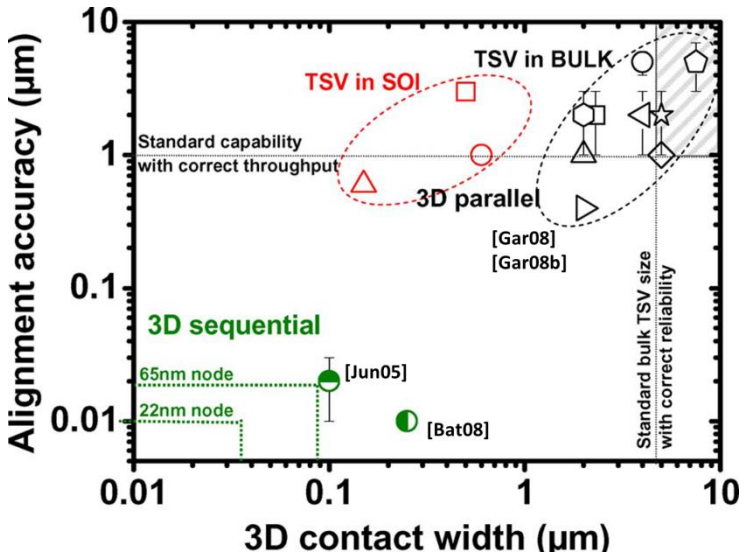


Figure III.1.1: Alignment accuracy variation with respect to contact width for parallel (hybrid) and sequential (monolithic) 3D integration [Bat12].

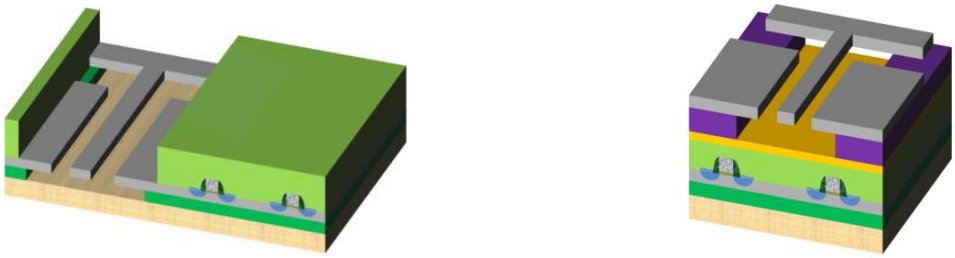


Figure III.1.2: Schematic representation of 2D and 3D M/NEMS-CMOS co-integration.

Direct metal-oxide bonding (described in section II.1.3 of chapter I) is an interesting alternative since a few numbers of steps are necessary to do it. Furthermore, W2W integration is possible involving a high throughput of production, and low resistance interconnection can be manufactured with a low pitch. The major issue of this approach is the high alignment requirements, since metallic pads have to be in regards to ensure an optimal electrical contact (see section III.1.3 of chapter 1).

Unlike some hybrid approaches, monolithic integration allows a better signal transmission as observed in chapter II. Performing resonator structures in c-Si can imply a front-end approach by using the monocrystalline silicon top layer of an SOI substrate, like in chapter II. This approach however requires precaution during release process, particularly the use of an aperture through the stack and a protective layer for both transistors and metal interconnections. Moreover this 2D configuration (illustrated in Figure III.1.2) may be area-consuming since the sensing part is located along the CMOS circuit, implying a minimal safety distance between these two blocks because of the release process (see chapter IV). All these parameters affect the NEMS pitch.

To overcome this issue, resonators can be processed on top of the circuit adopting thereby a 3D configuration (Figure III.1.2). As observed in the third part of chapter I, neither the middle-end, nor the back-end, nor the standard above-IC using material deposition allow the use of c-Si as structural layer for the resonators. Another solution consists in combining both an above-IC approach and a direct bonding.

I.2 A promising approach using direct bonding

The mix between above-IC and direct bonding make possible the fabrication of NEMS in c-Si while keeping a high density of such devices at the same time. The main steps of the corresponding process flow are described in Figure III.1.3 and III.1.4. First of all, two wafers are necessary: one for electromechanical devices and one for electronic circuits, which can be manufactured by a foundry (see section III.2 of chapter I). An SOI wafer is selected for c-Si based nano-resonators fabrication. In this integration scheme, all the high-temperature steps necessary for the NEMS development like thermal annealing and LPCVD deposition are forbidden in intra or post-CMOS approach. A solution is to make these steps before the final assembly. The latter is performed through a direct molecular bonding (or direct oxide bonding). Next, the removal of both the silicon bulk and the buried oxide (noted BOX) from the SOI substrate is necessary to pattern the resonator and its interconnections.

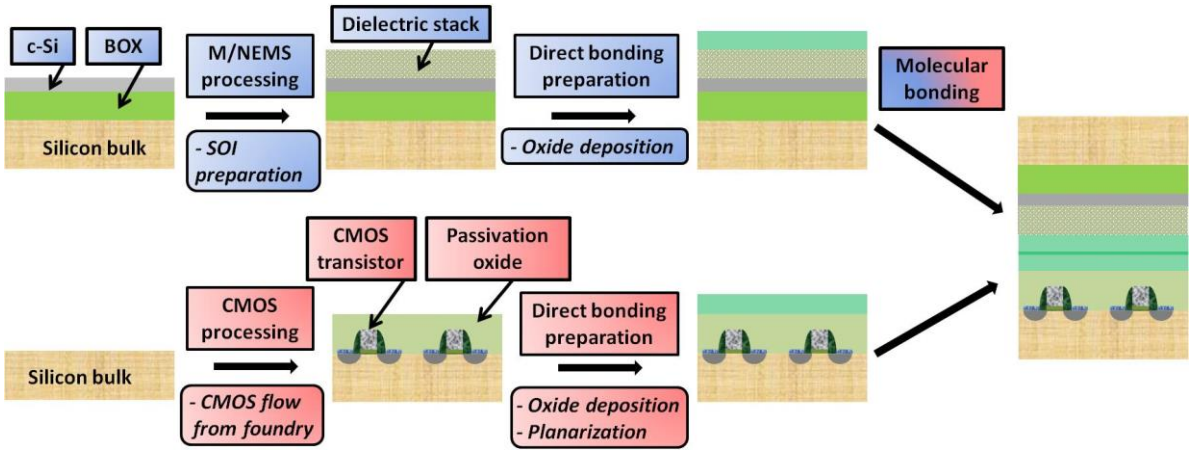


Figure III.1.3: Substrates preparation and direct molecular bonding constitute the first assembly steps. The nature and purpose of the dielectric stack will be detailed in sections II and III.

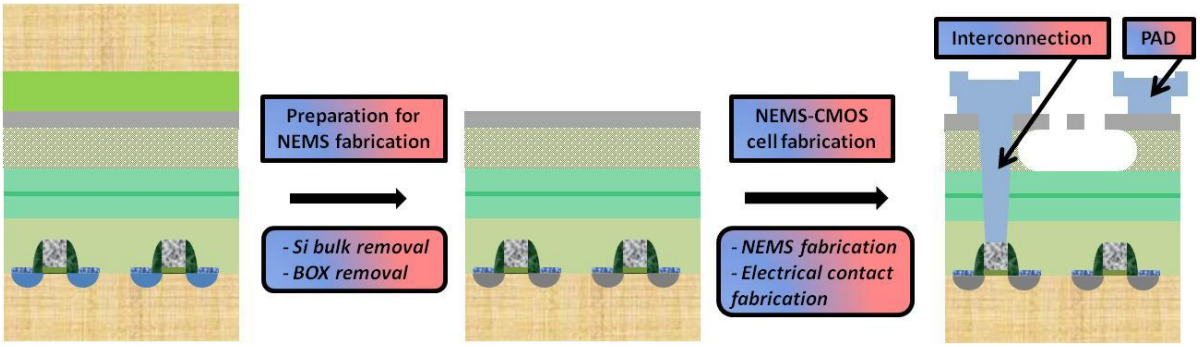


Figure III.1.4: Etching of silicon bulk and BOX from the SOI followed by the fabrication of both NEMS resonator and interconnection.

This summarized process flow description underlines some issues and interrogations. First, the NEMS device placement within the CMOS stack can be in ME or above BE, as illustrated in Figure III.1.5 (respectively in (a) and (b)). In a ME configuration, a shorter connection between both the sensing and the electronic parts is possible. Nevertheless such an approach requires stopping CMOS process flow after FE fabrication for molecular bonding step and electrical contact creation between transistors and resonators.

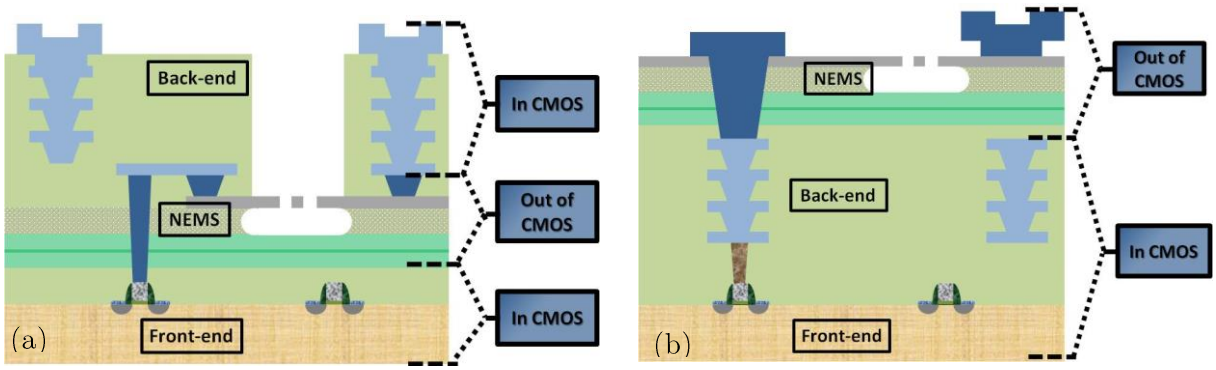


Figure III.1.5: Cross-sectional view of c-Si NEMS in ME (a) or above-IC (b) integration. The back-end here contains four levels of metal (in light blue). The indications on the right of each situation explain if fabrication occurs in or out of the CMOS process (respectively noted “in CMOS” and “out of CMOS”). Dark blue shapes correspond to the interconnections manufactured out of the CMOS process.

This strategy requires an expensive modification of the CMOS process. Furthermore, such a method implies an aperture to the mechanical structure through the back-end. A protection of interconnection during the mechanical release is also necessary. As presented in chapter II, this protection requires additional steps and masks contrary to an above-IC approach. Because of its low-cost and flexibility with respect to CMOS preparation, the latter is selected for NEMS array based sensor development. The development of such integration constitutes the main scope of this thesis

II. 3D NEMS-CMOS process flow

The previous section depicted two different 3D approaches based on a wafer-level molecular oxide bonding between CMOS and NEMS substrates. The strategy selected for this thesis will consist in processing the NEMS resonators above both the CMOS circuit and the interconnections. This section first proposes to define the main fabrication steps used in this integration before a fully description of the process flow.

II.1 Definition and characteristics of the main technological steps used in the developed process flow

II.1.1 – Lithography

It allows the shape definition of structures and requires two major elements: a resist (or photoresist) and a mask. Several methods exist according to the size of the device: electron-beam (or e-beam) lithography which uses electrons as radiation element for patterns sizes smaller than 100nm, and photolithography for bigger patterns performed with ultra violet (UV) or deep ultra-violet (DUV) light. Unlike the e-beam method directly performed from a computer through CAE (Computer Aided Engineering) software, photolithography operation requires a mask. The latter comprises a glass plate with a patterned opaque layer (typically chromium) on its surface, corresponding to the motifs to be transferred on the polymer resist. In Figure III.2.1 is described a standard microelectronic photolithography process. The photoresist deposition is first performed by spin-coating on the material to be patterned. Next, this photoresist layer is exposed to UV (or DUV) light through a mask after a pre-alignment with the substrate. This alignment operation is allowed thanks to marks present on the substrate. Depending on the nature of the polymer (see Figure III.2.1), the exposed or unexposed photoresists areas are removed during the resist development. The remaining material will act as a protection for the next etching step.

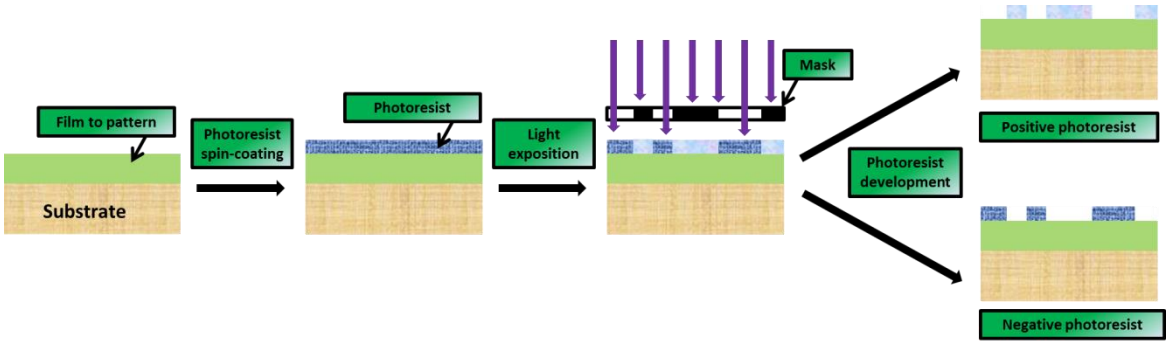


Figure III.2.1: Process flow of photolithography process.

II.1.2 – Etching

Etching operation allows an entire or local removal of material on a substrate (Figure III.2.2). In the second case, a photolithography is necessary to etch the material not protected by the photoresist. Two ways exist for this step: in wet or dry condition [Wol86-Run90]. In wet etching, the process occurs in a liquid chemical bath or with vapor etchant. It is commonly used for performing isotropic material removal (except in some cases, such as Si etching using KOH agent). The dry option requires a plasma (partially ionized gas) in which etchant species are produced. In this case, an anisotropic etching occurs. This operation is usually used for the devices pattern on silicon (like transistors and M/NEMS) and for metallic interconnections fabrication. For much deeper via construction, for example in TSVs fabrication, another approach consists in using RIE (Reactive Ion Etching) technique in which another more reactive ionic gas (e.g. sulfur hexafluoride for Si etching) is added. The particles from this ionic gas are then sputtered on the surface of the substrate thanks to a high voltage and allow a deeper etching. After this step, the photoresist is removed thanks to a stripping operation.

For surface micromachining, the control of etching process is crucial. This can be performed by adjusting the etching duration according to the etch rate, or by using a layer less reactive located below the material to be etched. Selectivity is thus an important parameter for this step. It characterizes the etching process and corresponds to the etch-rate ratio between two different species. Moreover, the photoresist can either or not react with the chemical agents. So, according to the etching selectivity between the material to pattern and the photoresist, a sufficient thickness has to be deposited in order not to damage the protected areas.

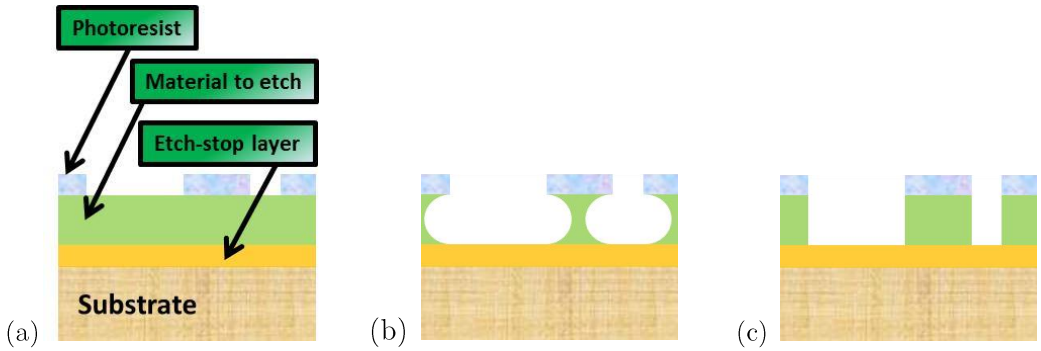


Figure III.2.2: Schematic of isotropic (b) and anisotropic (c) etching after photolithography (a).

II.1.3 – Doping

Doping is used to modify the electrical conductivity of a semiconductor. Some impurities are introduced inside it and affect its band structure and so its electronic properties. Several method exist for this purpose (diffusion, neutron transmutation, laser), but ionic implantation is commonly used in microelectronics. Impurities are sputtered from a source onto a target thanks to electromagnetic fields. This technique allows a control of the dose and of the implantation energy of the dopants, which respectively affect the number of impurities and the depth localization of them inside the semiconductor. These parameters have an influence on the electronic behavior of the material. According to the nature of the impurities, material can have either more electrons or more holes, *i.e.* can be respectively n-type or p-type. For silicon, the most used dopants are boron (B) to add holes and phosphorous (P) or arsenic (As) to add electrons. A higher concentration of these impurities brings more charge carriers and improves semiconductor electrical conductivity.

This doping process is usually used to build transistors (source and drain formation), to improve the contact resistance and to modulate the gauge factor of M/NEMS resonators, as explained in [**Kan82-Smi54**]. After implantation, the crystallographic structure of material is modified and damaged due to the dopants insertion. In order to restore it and activate these dopants, a thermal annealing is required.

II.1.4 – Thermal annealing

In this step, samples are exposed to high temperatures for a defined duration. Thermal annealing process is used for several reasons: silicon oxide growth, recrystallization of structures, dopants diffusion and activation in semiconductors and preparation of substrates to high thermal budget. An oven is commonly used for these operations, but thermal annealing via laser is also possible.

II.1.5 – Material deposition

Material deposition is necessary for electronic devices fabrication. Three particular kinds of materials are commonly used: dielectrics (oxides, nitrides), metals (one element or alloy) and semiconductor (e.g. amorphous Si, poly-Si, poly-SiGe etc). The most common techniques are Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD), allowing a deposition in the range of tenths of nanometers up to few micrometers. These processes are generally performed at low pressure (some mbars or less).

PVD uses evaporation or sputtering of a solid source whose particles are then deposited on the substrate. After that, nucleation and coalescence phenomena lead to the film growth. Evaporation or sputtering can be performed through thermal, electron beam, cathodic arc, pulsed laser methods and so on [Ses02-Ros90].

CVD uses the species created inside a gas or vapor for the deposition. This can occur at atmospheric (APCVD), low pressure (LPCVD) or with plasma (PECVD). In CVD process, chemical reactions on the surface substrate are at the origin of the films formation. APCVD and LPCVD generally require temperatures above 500°C (depending on the material to deposit) whereas temperatures below 500°C are used in PECVD approach. Unlike PVD, CVD allows conformal deposition: almost the same thickness is present on the substrate whatever the surface topography.

Electro-Chemical Deposition (ECD) is a technique especially used to make copper interconnections. The substrate is first coated by the material to deposit, followed by electrolysis of a solution containing the desired metal ion or its chemical complex.

II.1.6 – CMP

Chemical-Mechanical Planarization (or CMP) is a commonly used process for back-end fabrication. Its goal is to smooth a surface with the combination of chemical and mechanical forces. The process requires an abrasive and corrosive chemical colloid called slurry; a polishing table; a wafer carrier and a pad conditioner (see Figure III.2.3). The substrate to flatten is placed on the carrier and pressed to the polishing table. Both table and carrier are driven rotating in the same direction unlike pad conditioner. With the slurry deposition, this conditioner modifies both shape and surface of the table, and thereby the sample surface. Different kinds of slurry are used according to the nature of the material to flatten (oxide, metal or semiconductor). This operation is often performed either in order to limit surface topography of a substrate and/or to decrease the thickness of a film (Figure III.2.4).

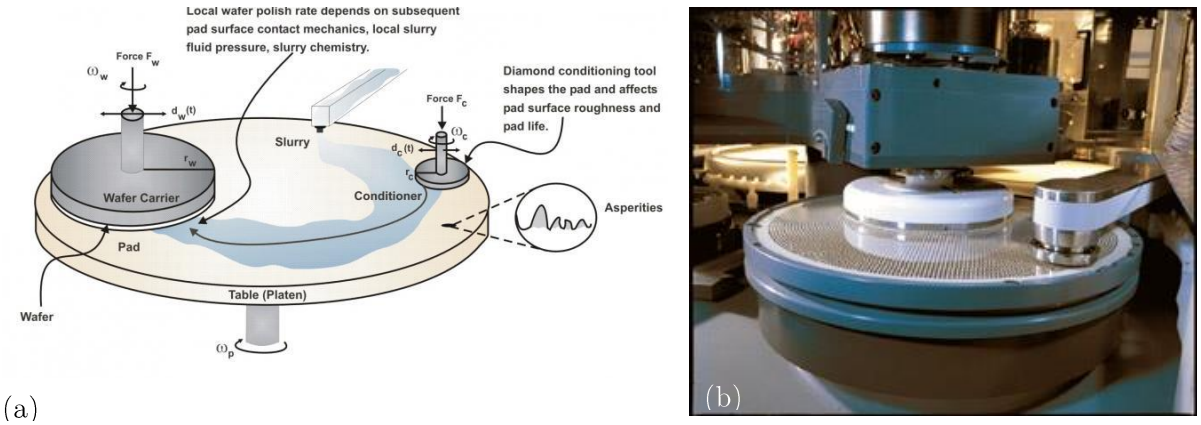


Figure III.2.3: Schematic (a) of a planarization process [SCS] and photography (b) of a CMP machine [BUS]).

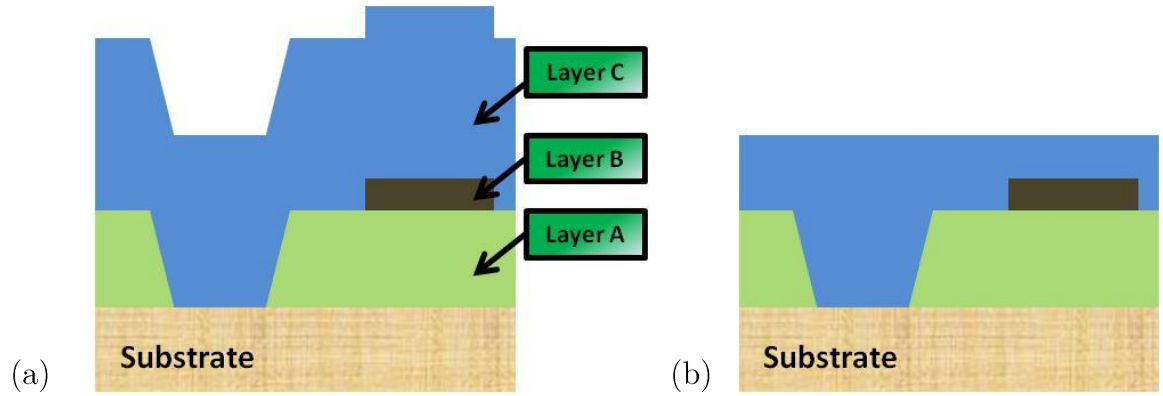
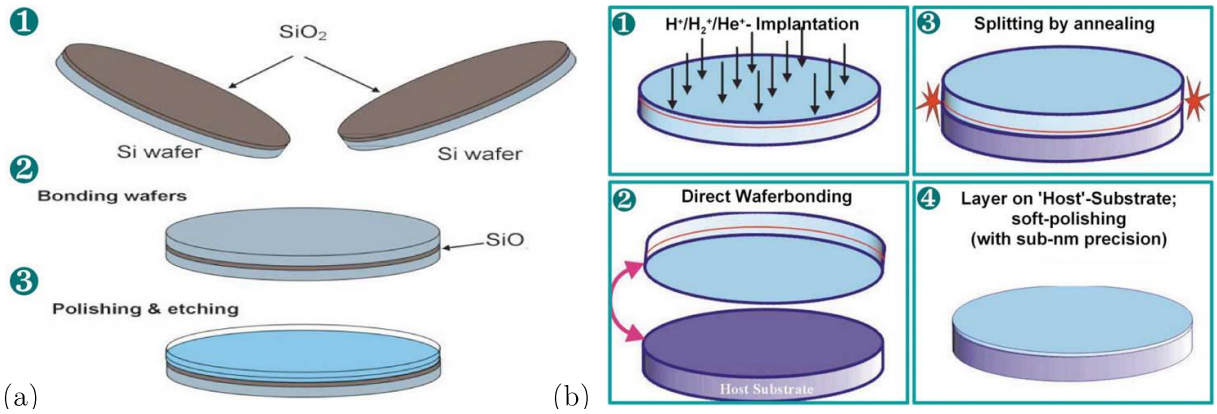


Figure III.2.4: Schematic illustration of a wafer with three different layers before (a) and after (b) CMP process.

II.1.7 –Direct wafer bonding

Direct wafer bonding was briefly depicted in the section III.1.3. Contrary to adhesive bonding [Nik06], it consists in attaching two materials by chemical bonding without any external adhesive. Several direct bonding techniques using different materials exist, such as hydrophobic or hydrophilic Si-Si, III-V materials; SiO_2-SiO_2; Cu-Cu; Al-Al; W-W; Ni-Ni bonding etc., making this step versatile [Mor12-Tan12-Li08]. This operation usually occurs in ambient air at room temperature and requires a high level of flatness and cleanliness of both substrate surfaces. Consequently CMP and cleaning steps are performed before bonding. After that, wafers are put together and chemical bonds are created. Then, as described in Figure III.2.5 (a), the bulk part of one substrate can be removed by polishing and etching. Bonding energy must be strong enough to resist to these steps, more particularly to the bulk reduction one. That is why additional thermal annealing and activation by plasma treatment (in UV-ozone environment for example) are performed during bonding process. The more the annealing temperature is, the higher the bonding energy is and so the better the bonding interface is.

Direct bonding is at the origin of the famous smart-cut process (Figure III.2.5-b) used by SOITEC© for SOI wafer manufacturing [Cel03].



(a) (b)

Figure III.2.5: Schematic of a typical wafer bonding process flow between two Si substrates partially oxidized (a) and illustration of the use of direct bonding for the smart-cut process allowing the creation of SOI wafers (b) [Chr06].

II.1.8 – Grinding

Silicon bulk thinning usually comes after direct bonding. It can be obtained either chemically through etching (with KOH or TMAH for example) or mechanically through grinding technique. The latter is commonly used for TSVs fabrication (see section III.1.4 of chapter I) and allows a reduction of silicon bulk thickness from almost 700µm to around 20-40µm. As presented in Figure III.2.6 (a), a wheel and the substrate are spinning in the same direction. The contact between the wheel and the wafer is located on the cm-size abrasive segments (Figure III.2.6 (b)) which will remove the material during the process. These segments are made up of grains whose nature differs according to the material to thin. An optimization of the grinding quality is possible by modifying the speed rotation and the tilt of sample and wheel. Two grinding steps are commonly performed: a rough polishing and a final polishing. The first one uses abrasive segments with ten micron size grains and has a thinning speed close to 100µm.min^{-1}. Its goal is to remove a large quantity of bulk material. The last one uses abrasive segments with some micron-size grains and has a thinning speed close to 20µm.min^{-1} in order to reduce topography and roughness at the wafer surface after rough polishing.

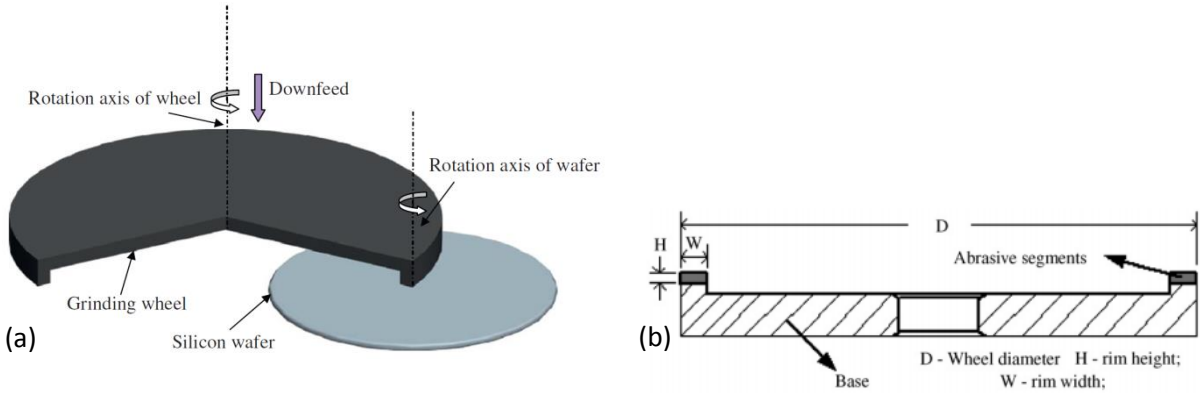


Figure III.2.6: Illustration of a grinding process (a) [Pei08] and cross-sectional representation of a grinding wheel (b) [Liu07].

II.1.9 – Profilometry

Profilometry is a measurement method allowing the determination of the profile, topography and roughness of a surface. This technique uses a stylus (commonly made in diamond) moved laterally in contact with the sample surface. The displacements of this stylus give information about the surface profile. Several ways exist to detect these displacements. An example using optical method is illustrated in Figure III.2.7. The force applied by the stylus on the sample and the move speed allows an optimization of the topography and roughness measurement according to the material and the surface state of the sample.

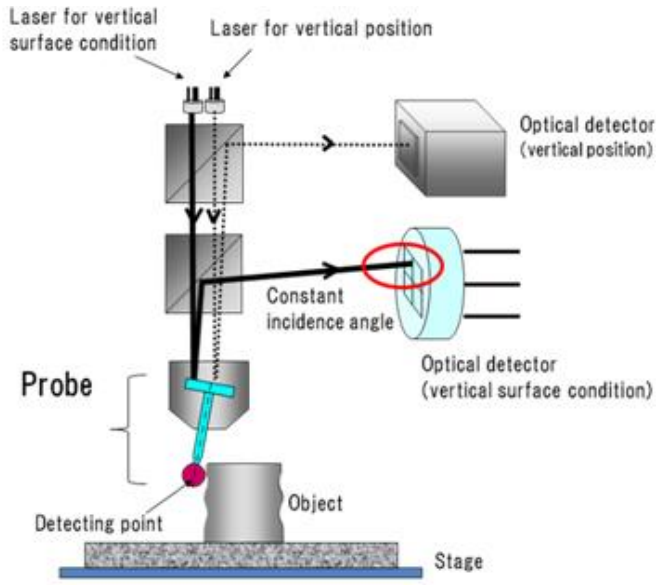


Figure III.2.7: Illustration of a profilometer tool using an optical detection.

II.1.10 – Ellipsometry

Ellipsometry consists in measuring both the thickness of a material, present alone or inside a stack, and the optical indexes (refractive and absorption) of dielectrics. Basic principle is described in Figure III.2.8. A light source sends an electromagnetic radiation linearly polarized by a polarizer which falls onto the sample to characterize with an incidence angle Φ. After reflection, this monochromatic radiation passes through a polarizer (called analyzer) before reaching a detector. The use of a compensator (like quarter-wave or half-wave plate) for light treatment is optional. Both in-plane and perpendicular polarization components of the monochromatic radiation are used. The measurement of the amplitude and the phase

shift of these polarization states allow the determination of the thickness and the optical indexes. By modifying the incidence angle and the wavelength during characterization, it is possible to determine with more precision the thickness of the material.

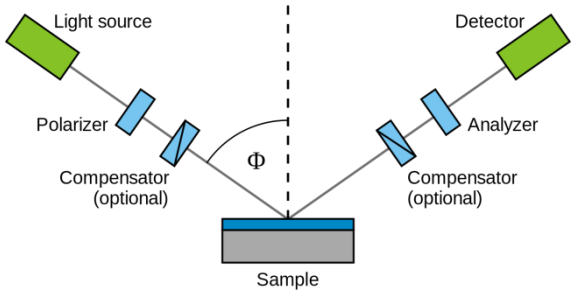


Figure III.2.8: Schematic setup of an ellipsometric equipment and experiment.

II.1.11 – Scanning acoustic microscopy

Scanning Acoustic Microscopy (SAM), or Acoustic Micro Imaging (AMI), is an observation technique used particularly for bonding interface analysis. This technique is based on the monitoring of the propagation and reflection of an acoustic wave (generally ultrasound) inside a stack as described in Figure III.2.9 (a). This wave is sent on a sample. As long as the acoustic impedances of the different stack components are the same, the ultrasound will continue to propagate inside the stack. However, if the impedance difference is strong (for example air and SiO_2), the acoustic wave is reflected and detected by the microscope. In this context, the detection of reflecting waves corresponds to a no bond area (Figure III.2.9 (b)) [Mar01]. On Table III.1 are depicted some longitudinal acoustic impedances.

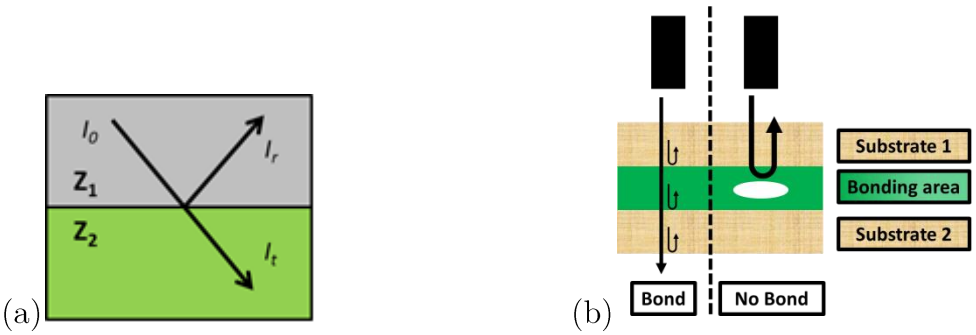


Figure III.2.9: (a) Illustration of the propagation of an acoustic wave inside a stack formed by two layers with different acoustic impedance Z_1 and Z_2. At the interface of this material, the wave I_0 is split into a reflective (I_r) and a transmitted (I_t) wave. (b) Schematic representation of SAM applied in direct bonding case.

Material	Longitudinal Acoustic Impedance (MRayl[15])
Si	~20
SiO_2	~13
Si_3N_4	~36
Water	~1.5
Air	~0.0005
Al	~17
Cu	~45
Ti	~27

Table III.1: Approximate value of longitudinal acoustic impedances for some materials [OND].

II.2 Process flow description

With the definitions given in the previous part, it is now possible to build the process flow for the sensor fabrication which will be described in this section. In the scope of this thesis, a post-CMOS approach is selected for the NEMS above-IC co-integration development. As a consequence, the temperature during the process must not overpass the maximum thermal budget limit with the presence of the CMOS substrate: as presented in the first chapter, it is evaluated at 450°C conventionally for standard back-end. [Sed01] shows that higher temperature can be used, but with a limited duration in order not to degrade the metallic interconnections. This co-integration development is divided into three major steps: preparation of SOI substrates, preparation of CMOS substrates and final assembly.

II.2.1 – SOI substrate preparation

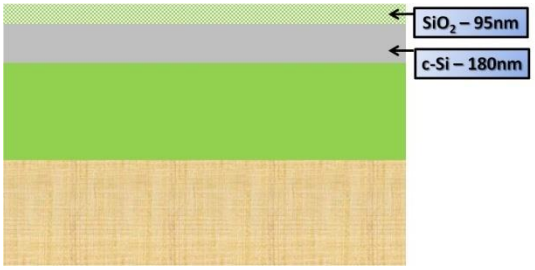
Figure III.2.10 illustrate step by step the preparation of the substrate dedicated to electromechanical devices fabrication. For the scope of the thesis, an SOI wafer is required as it allows the use of the c-Si as structural material. Moreover, since a post-CMOS above-IC integration is selected, all high temperature processes (e.g. thermal annealing and material deposition) exceeding the thermal budget limit of the CMOS substrate must be performed before the final assembly. Consequently all these steps are used during the SOI wafer preparation.

[15] One rayl corresponds to one $kg.m^{-2}.s^{-1}$

1

SOI wafer with 400nm BOX and 205nm c-Si.

2



Thermal oxidation for further Si thinning (1050°C).

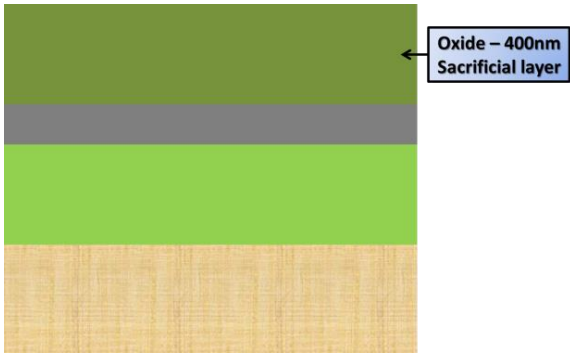
3

Wet etching of resulting thermal oxide layer (ambient temperature).

4

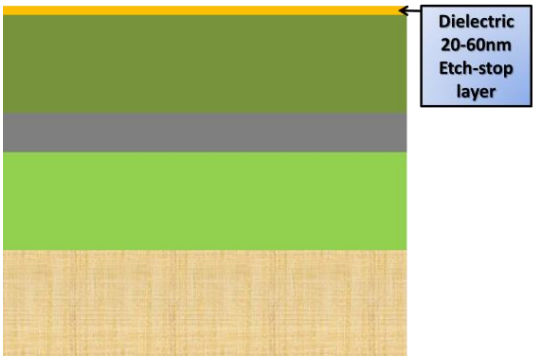
Doping with boron implantation and thermal annealing (800°C and 1050°C).

5



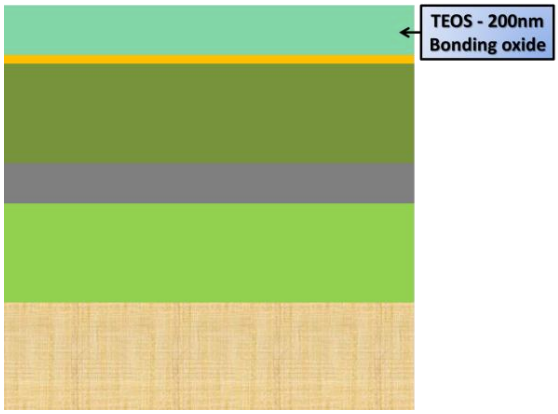
Oxide deposition for sacrificial layer definition (400nm) and thermal annealing (750°C).

6



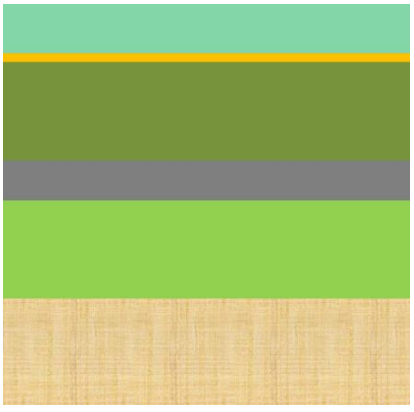
Dielectric deposition for etch-stop layer definition (20-60nm) and thermal annealing (depending on the material).

7



Oxide deposition as further bonding material (TEOS 200nm deposited at 400°C)

8



Bonding oxide dehydration through thermal annealing (400°C)

Figure III.2.10: Schematic of the process flow concerning the SOI substrates preparation

The thickness of the top c-Si layer is fixed at 180nm. To achieve this thickness, SOI substrates with a 205nm thick c-Si and a 400nm thick BOX are selected (1). A 90nm thick thermal oxide layer is formed with a thermal annealing performed at 1050°C for 15min (2), followed by a wet etching to remove the SiO_2 layer (3). This method is very accurate for the active layer thinning since the thermal oxidation phenomenon of silicon is well mastered and since the subsequent etching process removes oxide layer without any silicon consumption. As the tiniest c-Si pattern is evaluated at around 80nm, a 180nm thick top Si layer is selected in order to make easier the photolithography (this process is more detailed in section II.2.3). Indeed, such a thickness only requires a thin layer of photoresist, which is necessary to achieve this critical dimension of 80nm with a suitable reliability.

After that, the active layer doping is performed in order to optimize the gauge factor and thereby the piezoresistive transduction. Boron atoms (B) are implanted with a 20keV energy and with a dose of 1.10^{15} cm^{-2}. These parameters are chosen in order to obtain a doping level near 7.10^{19} cm^{-3} inside the silicon. Substrates are then annealed through two thermal treatments: a first one at 800°C for 30min followed by a spike annealing at 1050°C for few seconds, all in nitrogen (N_2) environment (4). These annealing processes are performed for impurities diffusion in the entire top silicon layer, for the recrystallization of the latter and for the dopants activation.

For the mechanical structures release, a sacrificial and an etch-stop layer are required. The characteristics of these materials will be investigated in section III.1. The sacrificial material requires a thermal annealing after deposition for outgassing and reinforcement. This step is performed at 750°C during 1h in N_2 atmosphere (5). An annealing operation is also necessary for the etch-stop material. According to its composition, the process is different (see section III.3.2) (6). A 200nm thick TEOS oxide is then deposited at 400° (TEOS stands for tetraethyl orthosilicate) (7). This TEOS material constitutes the bonding oxide and must be prepared carefully. For this, a thermal annealing at 400°C for 2h is performed in order to remove the water present inside the material (8).

II.2.2 – CMOS substrate preparation

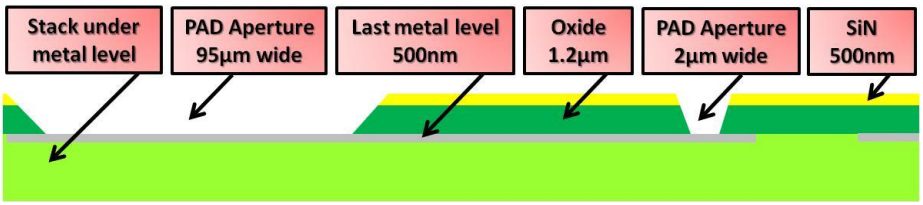
CMOS substrates preparation (manufactured in a foundry) is made in parallel of the NEMS wafers one. In the frame of this thesis, an AMS 0.35µm technology with four interconnection levels in Al was selected. Figure III.2.11 (1) symbolizes the CMOS wafer with its last metal interconnection level and some pad apertures (1). As described in Figure III.1.5-b, the co-integration strategy selected for this thesis consists in performing a direct bonding between SOI and CMOS substrates, thus requiring a

high planarity. As a consequence, the apertures at the CMOS wafer surface must first be filled by metal in order to make easier the interconnection process during the assembly (see II.2.3). This filling operation is presented here. In a first step, a pre-clean and a TiN-Ti barrier deposition (2) are performed. The pre-clean corresponds to a slight etching of Al surface in order to remove the native oxides for improving the electrical contact. PVD (20nm of Ti and 20nm of TiN) and CVD (20nm of TiN) depositions are performed. After the barrier formation, another pre-clean is made followed by a Cu PVD and CVD (respectively 50nm and 150nm) (3). The latter constitutes a seed layer for the ECD Cu which is electroplated until a 2.2µm thickness. After a reinforcement annealing, a CMP of Cu is processed until reaching the SiN back-end layer (4).

A Ti-based barrier is necessary in CMOS technology. It allows a better adherence of metallic interconnects and avoids metal diffusion in the back-end passivation. In this integration, Cu must be encapsulated to prevent any migration. Therefore, a 80nm thick TiN layer is deposited by CVD and PVD techniques (5), followed by lithography and etching to define the Cu encapsulation (6). This layer will also limit alignment problems during interconnection fabrication between NEMS and back-end (more detailed in the subsequent section). Etching is stopped at the SiN layer level.

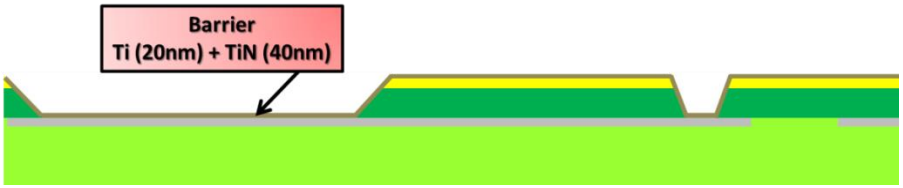
The deposition of a 500nm thick TEOS oxide (7) is followed by a planarization step to achieve a 200nm thickness. The final 2h long 400°C dehydration annealing constitutes the last steps for the CMOS substrates preparation before the direct bonding (8). All this process flow respects post-CMOS temperature requirements.

1

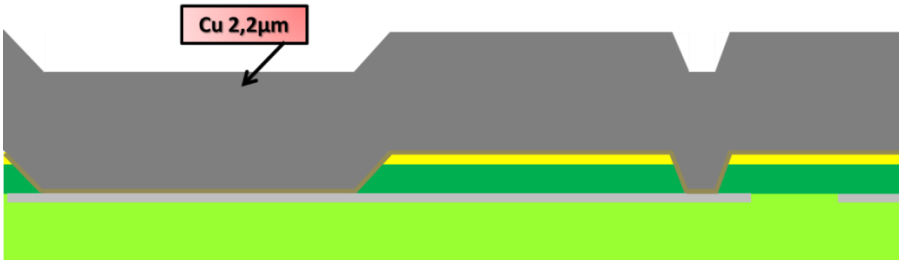


Schematic of a CMOS wafer with access to the last metal level used for the co-integration implementation.

2

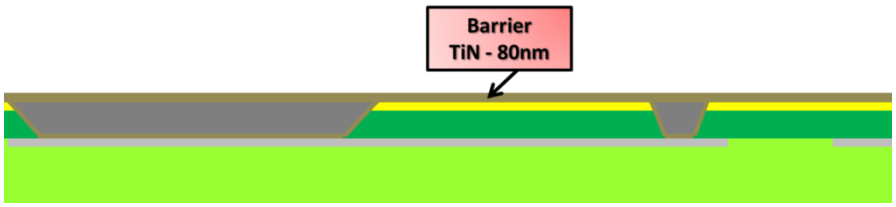


PVD and CVD Ti-TiN barrier deposition (380°C maximum).



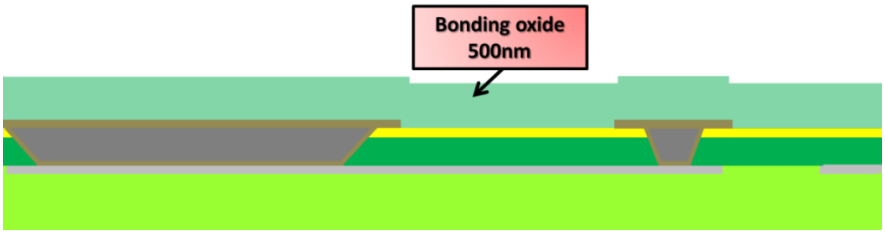
3 PVD, CVD and ECD Cu deposition (ambient temperature) and thermal annealing (250°C maximum).

4 Cu and TiN planarization (ambient temperature).

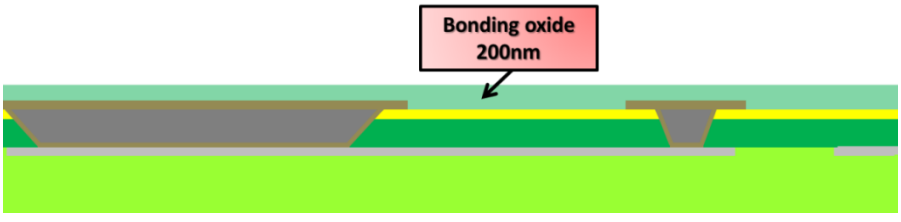


5 CVD and PVD TiN barrier deposition (380°C maximum).

6 DUV lithography and etching of TiN barrier (ambient temperature).



7 Bonding oxide deposition (TEOS deposited at 400°C).



8 Oxide planarization and dehydration through thermal annealing (400°C).

Figure III.2.11: Schematic of the process flow for CMOS wafers preparation.

II.2.3 – Final assembly

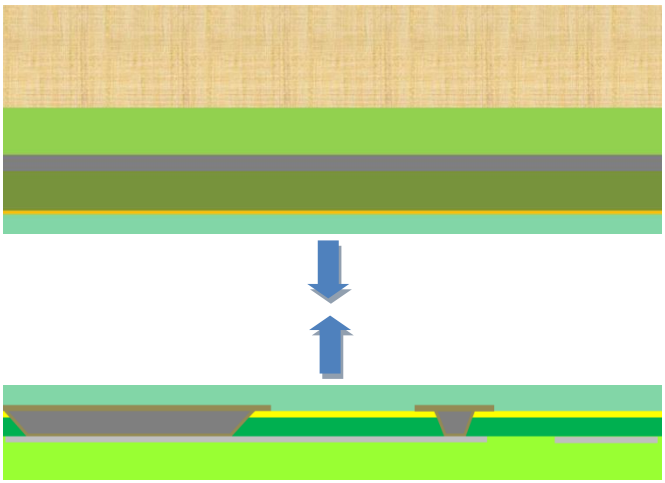
After the preparation of both base-wafers, the final assembly can be performed. This step is depicted in Figure III.2.12. After a dehydration annealing, a slight planarization, which consists in removing few nanometers of material, is performed before the molecular bonding. Both oxide surfaces are put in contact. As said in II.1.7, this step occurs at ambient condition in N_2 plasma. At the end, a 400°C thermal annealing for 90min in N_2 atmosphere is performed in order to consolidate the bonding.

In order to fabricate the nano-resonators, an access to the c-Si layer is necessary. A first grinding made by a rough polishing is applied to reduce the silicon bulk thickness down to almost 40µm. The remaining silicon material and BOX must then be removed. An easy method would consist in using an isotropic TMAH etching for silicon and an isotropic liquid HF (hydrofluoric acid) etching for oxide. But in this case, an anisotropic method will be used to avoid any damages of bottom and lateral sides of the wafers.

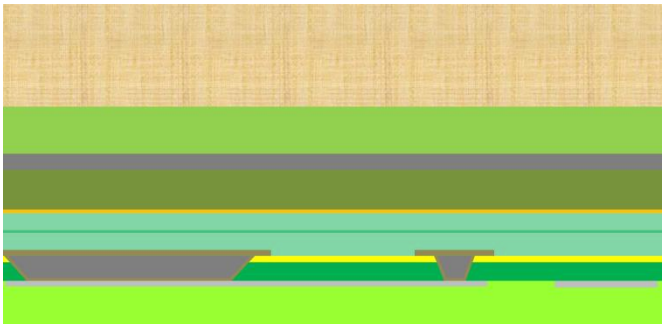
Even if the materials above the c-Si are removed, NEMS devices cannot be fabricated. Indeed, an alignment between both wafers is first necessary. This step has a direct incidence on the future alignment between vias and CMOS pads (performed later in the process), which will impact on the electrical contacts between the sensing and the electronic parts. During the wafer bonding step, a pre-alignment using the notch of each substrate is performed. Its millimeter precision is too low for ensuring a correct alignment. For this purpose, some alignment marks called Primary Marks (PM) are performed during the CMOS and the back-end process. Such marks are located like depicted in the Figure III.2.13 and have a typical dimension around 100µm.

Figure III.2.14 describes the resonators and interconnections fabrication process. This figure is divided into eleven blocks representing the different steps. Each step comprises four other blocks: the upper ones correspond to top views of substrate and lower one to cross-sectional view according to the arrows present in top view. The schematics on the left deal with field areas of the die where devices are defined and schematics on the right report on the fabrication steps of periphery area. The latter is made up of different patterns allowing different measurements, such as lithographic masks alignment, material thickness' determination and so on. All these different zones are depicted in Figure III.2.13.

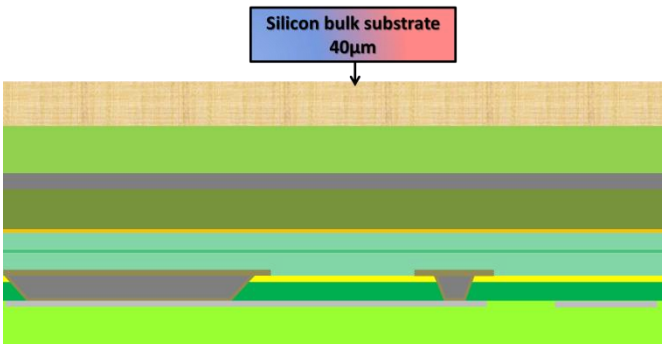
Since a 180nm thick c-Si layer is not fully transparent, the silicon present just above the PM is removed through lithography and etching operations (step 1). Because of its transparency, the dielectric stack etching is not necessary.



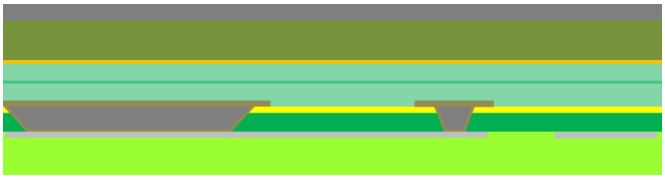
1 CMP touch up for both substrates and preparation for the bonding (ambient temperature).



2 Molecular bonding and thermal annealing (400°C).



3 Silicon bulk grinding (rough polishing at ambient temperature).



4 Silicon and BOX anisotropic etching (ambient temperature).

Figure III.2.12: Schematic of the process flow for bonding and silicon thinning.

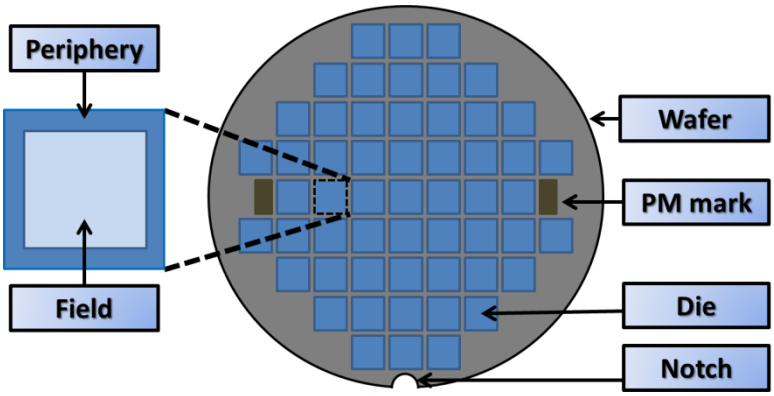
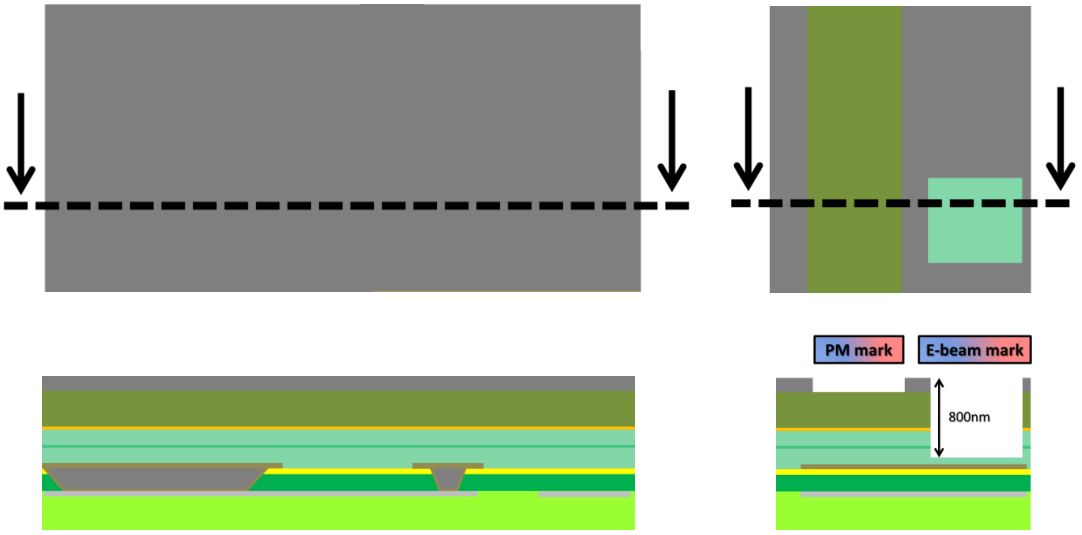


Figure III.2.13: Schematic of a wafer and die description. The devices are defined in the field part. The different patterns to measure the masks alignment, material thickness' are performed in the periphery.

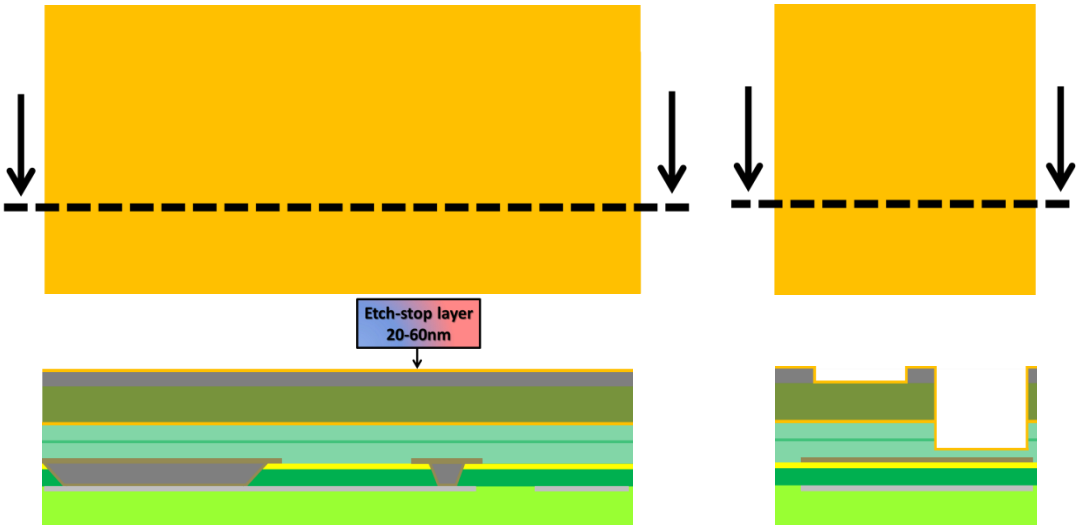
After the PM opening step, some lithography and etching operations on c-Si layer are then performed. This layer is patterned by a hybrid lithography step combining an e-beam lithography to define the resonators and a 248nm DUV lithography to define future above metallic routing, vias and pads (step 4). In this thesis, a specific resonator is used as test vehicle: its dimensions are depicted in Figure III.2.15 and Table III.2. To perform the e-beam lithography, the pattern of particular marks on each die is necessary. E-beam lithography machines need indeed these marks to correctly place the NEMS patterns in the field. These marks are located in the periphery zone (Figure III.2.13), have a size of 10µm x 10µm and are 800nm deep. This means that the etch-stop layer is removed in these areas, impacting on the underlying stack integrity (*i.e.* bonding oxide and back-end layers) which is not protected from the final NEMS release step. Consequently, a thin layer of etch-stop layer is deposited and etched everywhere except on these particular areas (steps 2 and 3).

After silicon etching, the metallic vias, routings and pads are created. This starts by a passivation layer deposition and planarization (steps 5 and 6). The nature of this material is studied in the next section. Some lithography and etching processes are then made on this passivation layer allowing both metallic routings and electrical contact between top silicon layer and Cu definition (step 7). Another similar step is required for the vias fabrication. An anisotropic etching is used to remove both the silicon layer and the dielectric stack until reaching the TiN barrier deposited during the CMOS substrate preparation (step 8). The process continues with a deposition of metal for the electrical contact definition between TiN barrier and c-Si (step 9). The choice of this metallic material will be discussed in the next section. The last DUV lithography and etching steps are performed to define metallic pads and lines (step 10).

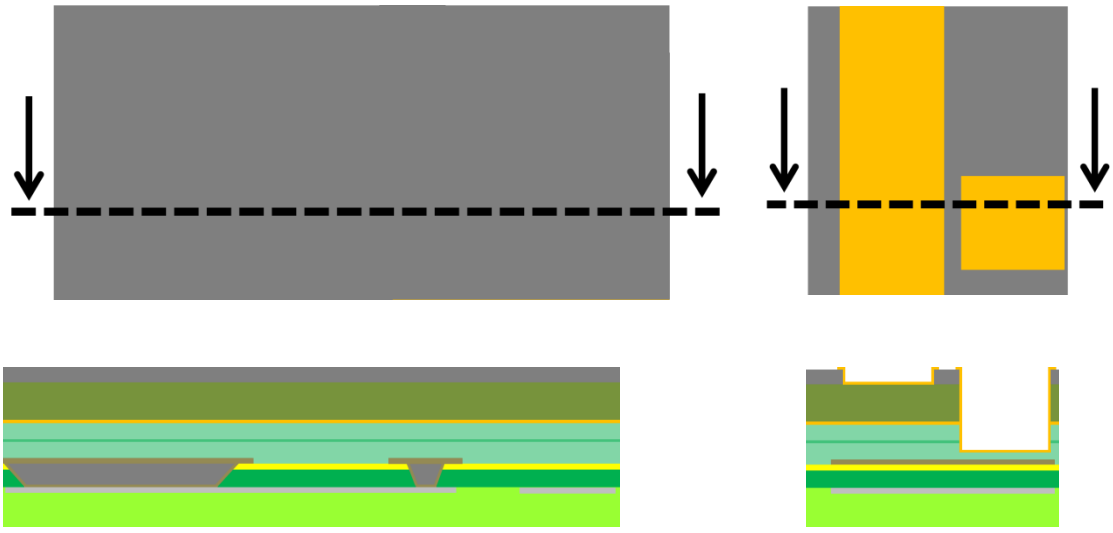
Finally, the mechanical structures are released (step 11) with vapor HF. Its goal is to remove all the oxide materials surrounding the resonators. The duration of this etching depends on the oxide materials and will be investigated in the next section. The etch-stop layer ensures the protection of the bottom part during HF exposition.



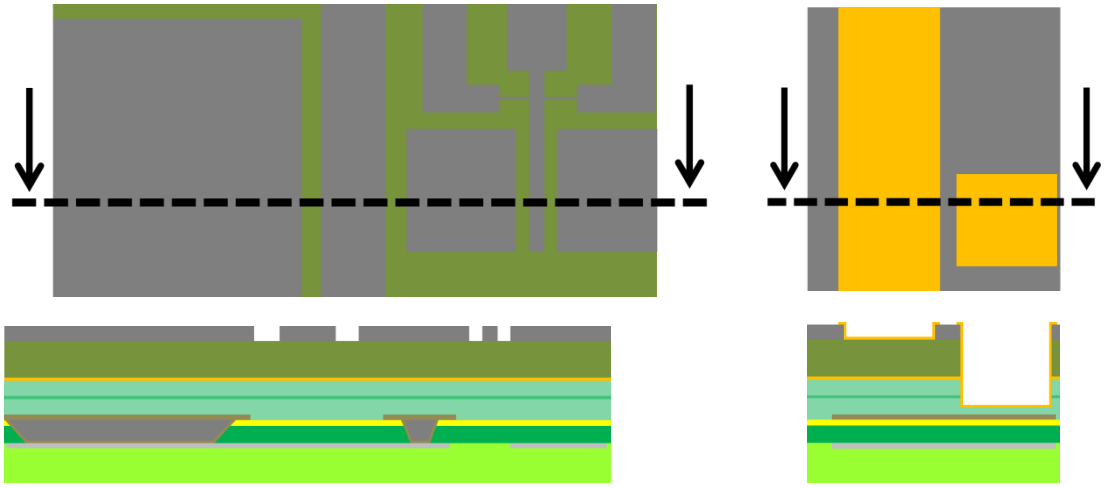
1 DUV lithography and etching of silicon for PM and e-beam marks.



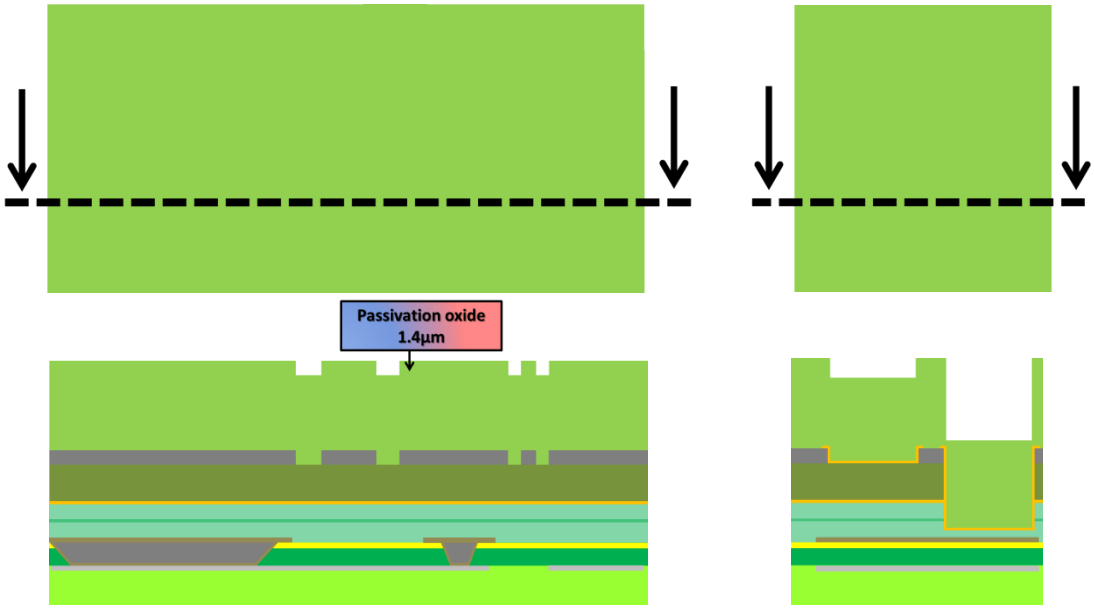
2 Etch-stop layer deposition (less than 450°C).



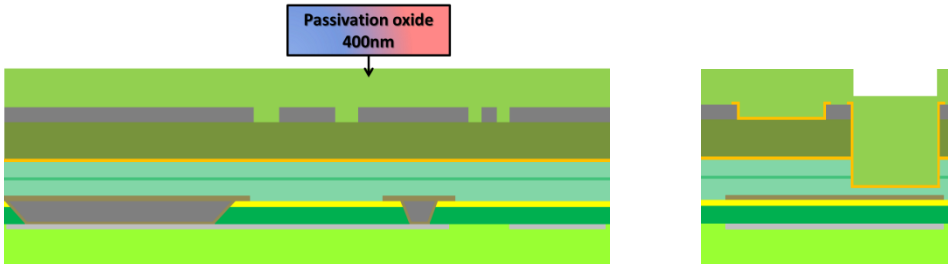
3 DUV lithography and etching of etch-stop layer.



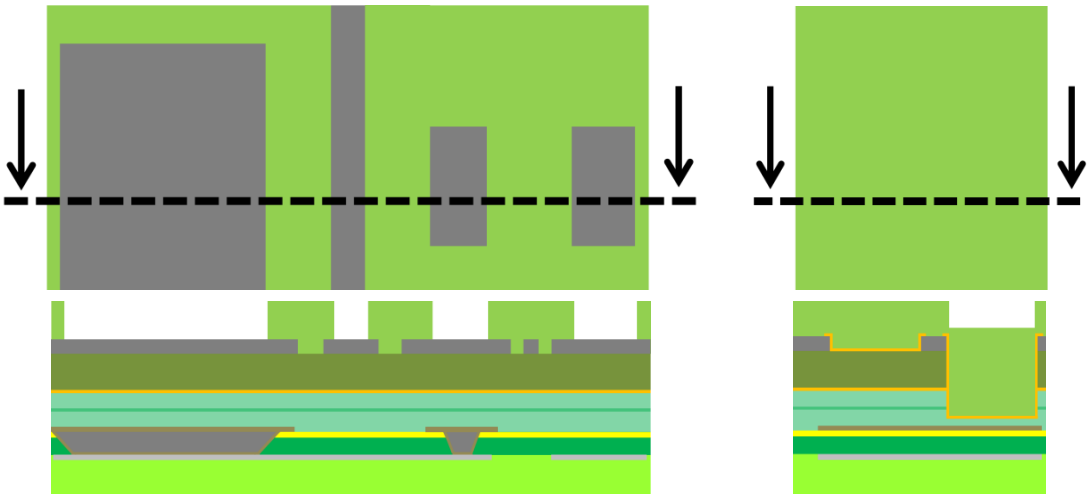
4 Hybrid lithography and etching of silicon to define the resonators and its metallic routings and pads (see 11).



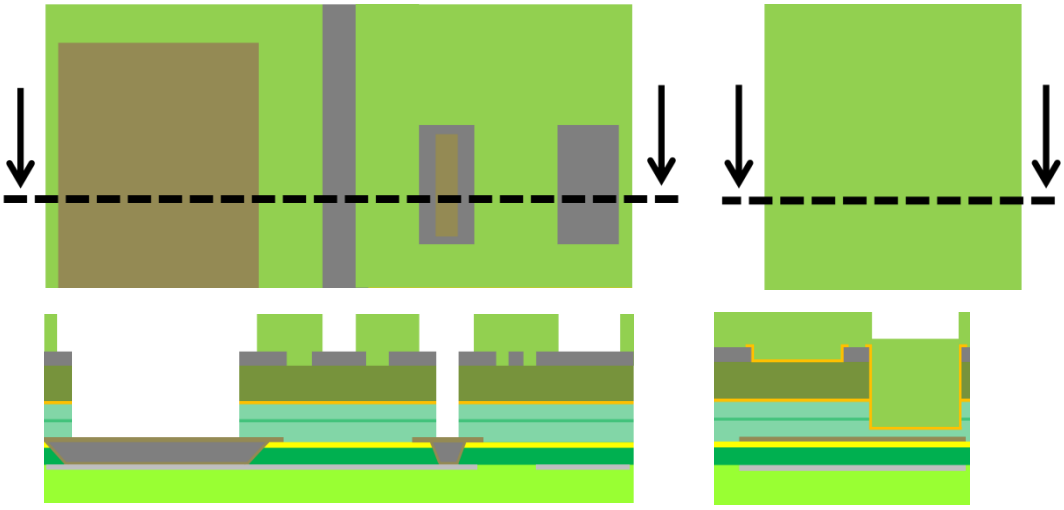
5 Passivation oxide deposition (less than 400°C).



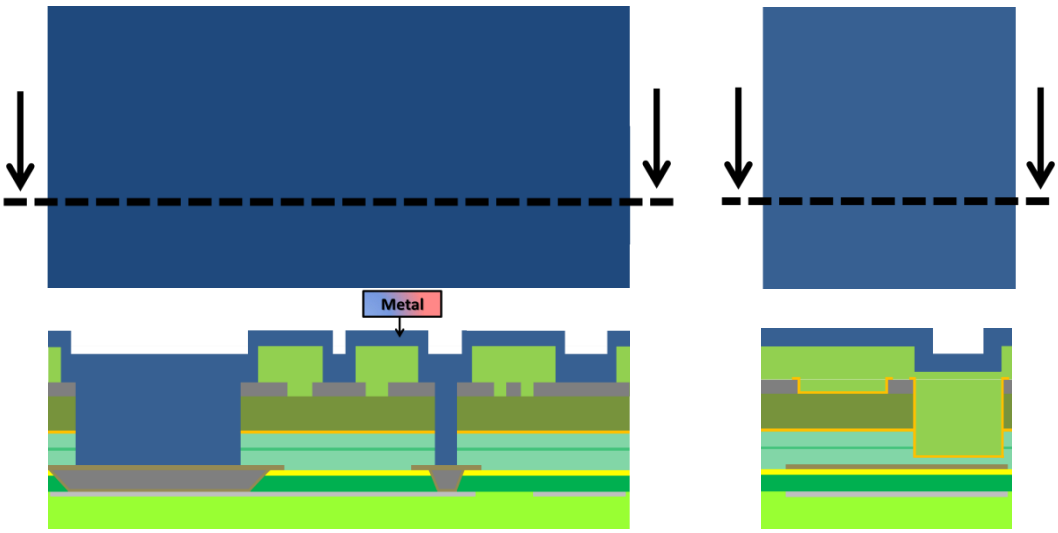
6 Passivation oxide planarization.



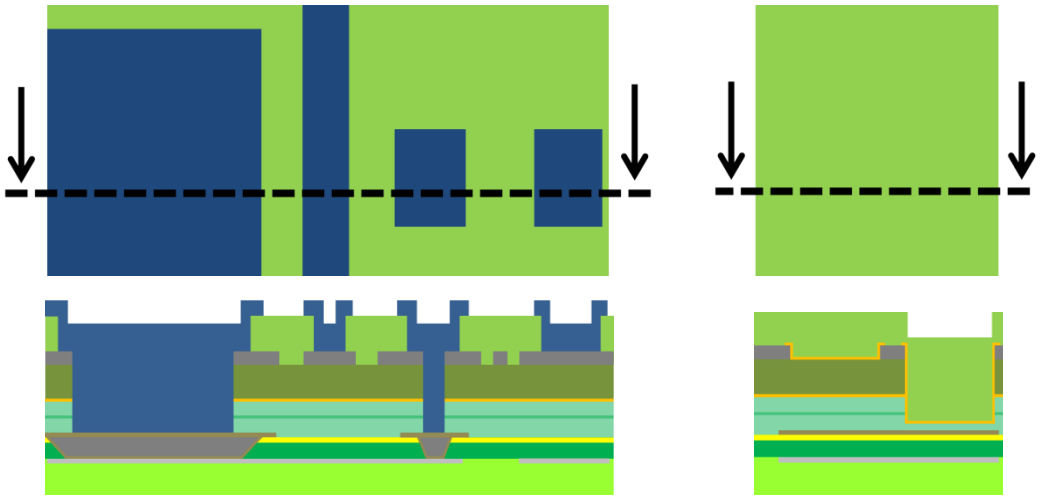
7 DUV lithography and etching of the passivation layer for metal pads, vias and routings definition.



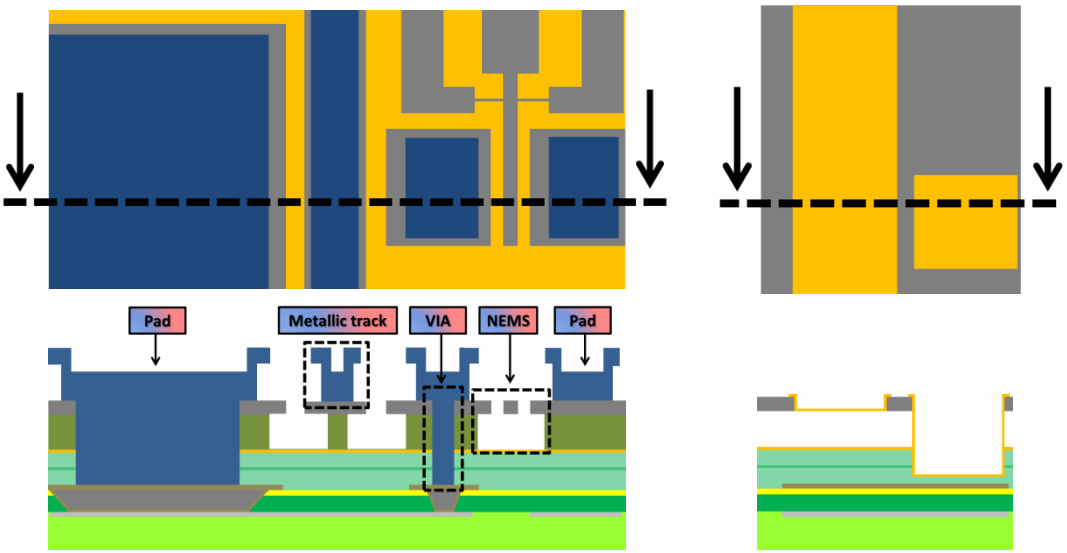
8 DUV lithography and etching of the silicon and dielectric stack down to Ti-TiN barrier for the metallic vias and pads fabrication.



9 Metal deposition (less than 450°C).



10 DUV lithography and etching of the metal layer.



11 Vapor HF etching and NEMS structures release.

Figure III.2.14: Schematic of the process flow for NEMS and interconnections implementation.

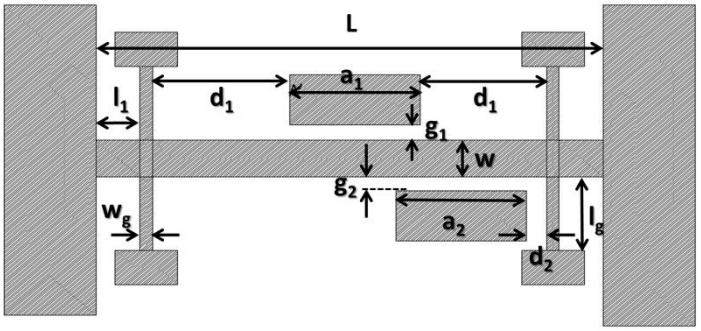


Figure III.2.15: Top view schematic of the test vehicle nano-resonator.

L	w	l_g	w_g	a_1	a_2	d_1	d_2	g_1	g_2
10	0.3	0.3	0.08	7.04	5	1	0.2	0.2	0.1

Table III.2: Test vehicle NEMS dimensions (in µm).

III. Technological modules study

The 3D NEMS-CMOS co-integration strategy proposed in the frame of this thesis provides some interesting features. Indeed, as resonators are fabricated after the assembly, low alignment requirement between the substrates is necessary. This step can be performed by the etching of c-Si in order to clear the large dimensions PM marks.

Concerning the release process, the use of an etch-stop layer has a positive consequence on the interconnections fabrication between the NEMS and the back-end. Instead of depositing a sacrificial layer thick enough to protect the underlying part, a thin material layer is here necessary, thus reducing the interconnections dimensions and so making easier their implementations.

In order to demonstrate this integration, three major technological modules (depicted in Figure III.3.1) have to be investigated:

- the molecular wafer bonding between the SOI and the CMOS substrates;
- the interconnection fabrication between the sensing part and the back-end;
- the NEMS release step.

These modules were studied in the frame of this thesis and will be further detailed in the following section.

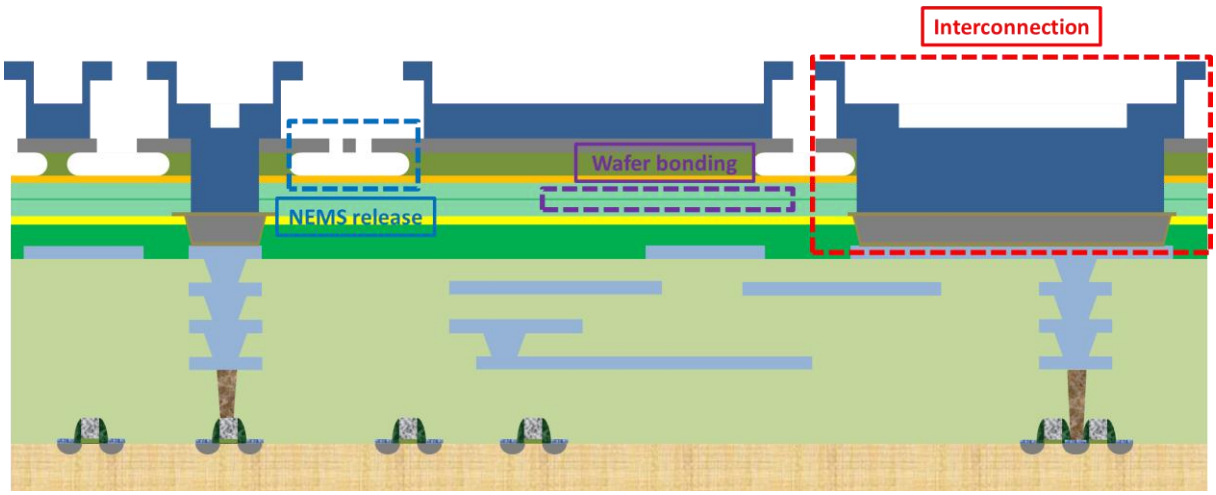


Figure III.3.1: Technological modules description of a 3D NEMS-CMOS above-IC cell.

III.1 NEMS release

This step constitutes the last operation of the process. It consists in etching all the oxides around the mechanical structure without damaging the resonator itself. A lot of studies around this problematic exist. [Wil96] reports on a wide variety of etchants according to various MEMS structural layers. For Si-based structures, the common method uses HF as etching agent because of its high selectivity with respect to silicon. The reaction between this etchant and oxides is explained in detail in [Kno00]. In summary, this reaction requires a catalyst (e.g water or alcohol) able to catch a proton from HF which will react with silicon oxides. At the end, one product of this reaction is water which is a catalyst of this reaction.

The release process is constituted by several steps: an exposition of the chemical agent to etch the oxide, a rinsing to remove the residues and a drying to clean up water. The most common way consists in doing the etching in a liquid HF batch, followed by a water rinse and an air drying.

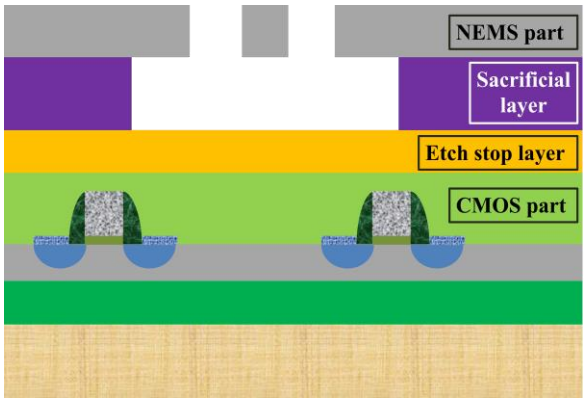


Figure III.3.2: Cross-sectional simplified representation of a NEMS in an above-IC configuration with the main layers of interest.

This process is interesting for MEMS structures, particularly when the gap between the resonating part and the substrate is high. However, the water produced during the reaction is at the origin of stiction phenomena constituting an important issue for nano-resonators integrity. Other solutions exist to avoid these adhesion problems: water presence removal thanks to supercritical carbon dioxide (CO_2) drying [Mul93-Bus94]; material coating of the mechanical structure to make the material hydrophobic, for example ammonium fluoride (NH_4F) [Hou95]; delaminating by vibrating method [Sav07] or by laser treatment [Kop05]. These techniques are however either technically difficult to apply, or expensive. For NEMS structures, the vapor HF etching using alcohol as catalyst appears as an optimal solution, and was studied by many research groups [Wit00-Yan06-Rit09-Pol13].

This solution greatly simplifies the release of nano-resonator devices: it drastically limits the water presence and avoids the use of complex rinsing and drying steps. According to the selected integration strategy, this type of release implies the selection of two kinds of materials. The first one is a sacrificial layer in order to achieve a well-controlled and clean release of the mechanical structure. The second one is an etch-stop layer located between the NEMS and the CMOS circuit to protect the latter (Figure III.3.2). A description of the experiments used for the morphological studies will be detailed here after, allowing the final material selection to develop this 3D co-integration approach.

III.1.1 – Experimental setup description

The substrates used for all experimental studies were 200 mm diameter (100) p-type silicon wafers. For the sacrificial material study, several Si-based oxides of different natures were studied by using a structure composed by an array of silicon beams covered by oxide. Both the fabrication process and the configuration are depicted in Figure III.3.3 and Figure III.3.4-a respectively. Dielectric oxides constitute potential sacrificial layers thanks to the well-known high selectivity of HF etching compared to silicon which is inert under vapor HF environment. A blanket deposition of material was used for the etch-stop layer study (Figure III.3.4-b). Two nitride-based dielectric materials and one hafnium dioxide (HfO_2) layer were studied in particular. All the materials used as sacrificial and etch-stop material are indicated in Table III.3 and III.4 along with the deposition process characteristics.

The materials selected for sacrificial layer study were deposited at a temperature below 450°C to be compatible with the back-end layer. Furthermore, this material is used both as sacrificial and passivation layers in order to keep the same etch-rate and so a more controlled release operation. High Temperature Oxide (HTO) deposited at high temperature is also studied for comparison with the other materials.

Some materials have been already investigated as etch-stop layer like alumina (Al_2O_3) and titanium dioxide (TiO_2) [Yan06]. High temperature nitride (HTN), well-known to be a protective layer during chemical etching, is a reference material for this study. Boron Nitride (BN) constitutes an interesting alternative. Indeed, its temperature deposition can be under 450°C and its deposition is very conformal (definition given in III.2) since it is deposited with CVD techniques. This material could also be used as protection after e-beam marks etching (see section II.3). The resistance of HfO_2 under vapor HF is also investigated. Because of its amorphous state just after its deposition, a rapid thermal process (RTP) up to 700°C for some minutes under N_2 atmosphere is necessary in order to crystallize it, since this material shows a better resistance in a monocrystalline state.

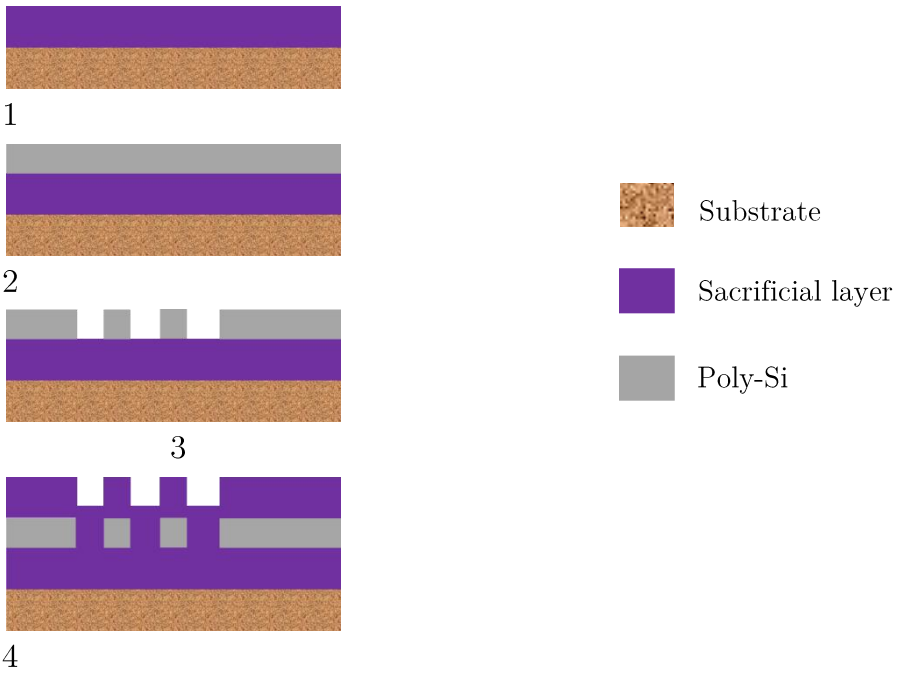
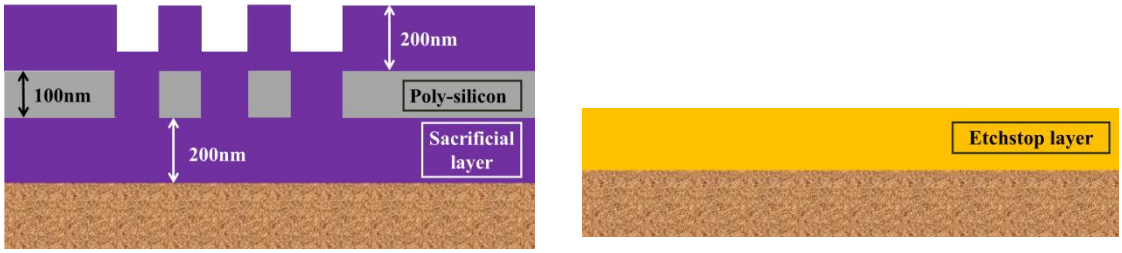


Figure III.3.3: Fabrication process for sacrificial layer study: (1) sacrificial layer deposition, (2) poly-Si deposition, (3) beams array definition and patterning, and (4) sacrificial layer deposition.

Material	**Growth method and Temperature (°C)**
Undoped Silicon Glass silane (USG)	PECVD / 270
Silane oxide (SiH_4)	PECVD / 400
Tetraethyl orthosilicate oxide (TEOS)	PECVD / 400
Tetraethyl orthosilicate Low Rate oxide (TEOS LR)	PECVD / 400
High Density Plasma Silane oxide (HDP SiH_4)	PECVD / 400
High Temperature Oxide (HTO)	LPCVD / 800

Table III.3:Material characteristics for sacrificial layer study.



(a) (b)

Figure III.3.4: Experimental setup for sacrificial layer (a) and etch-stop layer studies (b). Layer thickness in (b) depends on the etch-stop material. These two different stacks were placed under vapor HF environment.

Material	Growth method and Temperature (°C)
High Temperature Nitride (HTN)	LPCVD / 780
Boron Nitride (BN)	CVD / 480
Hafnium dioxide (HfO_2)	CVD / 400°C

Table III.4: Material characteristics for etch-stop layer study.

III.1.2 – Experimental results

Two parameters are critical for the selection of materials as sacrificial and etch-stop layers: the etch rate and the presence and dimensions of the residues, which may result from a silicon-fluorine complex precipitation during the etching process [Rit11]. Etching without residue is required to avoid any perturbation of the resonator's motion. Etch rates were calculated using ellipsometric measurements of the thickness before and after exposition under vapor HF. The results are presented in Figure III.3.5 and provide an estimation of the exposition time necessary to entirely etch the oxide present above and under the silicon beams. According to the configuration presented in Figure III.3.4-a, the exposition time required to etch all the oxide must vary between 37min and 56min, meaning that the etch stop layer material has to stay intact during this time.

After 10min of HF exposition, HTN etch rate is equal to 6 $Å.min^{-1}$. Even with this low etch-rate value this material cannot be used as etch-stop layer. However, BN and HfO_2 show the best resistance behavior with a zero etch rate even after respectively 80min and 2h of exposition. This resistance is confirmed on Figure III.3.7: their surface after etching is very clean contrary to HTN which presents some craters on the surface, potentially dangerous for the NEMS integrity.

The same morphological analysis was performed for several sacrificial materials (Figure III.3.8). The objective is to retrieve the oxide leaving the smallest amount of residues after vapor HF exposition. A 10min etching was applied on the different oxides studied. These observations show that TEOS, TEOS LR and HDP SiH_4 oxide constitute promising materials as sacrificial layer thanks to their very clean surface after exposition.

Nevertheless, residues present for SiH_4, USG and HTO can be removed after a rinsing step using water and a drying in an oven at 120°C for one hour (Figure III.3.9). However, the cantilever may collapse due to the water-induced capillarity effect which considerably damages the nano-resonators. This effect is shown on Figure III.3.9-b.

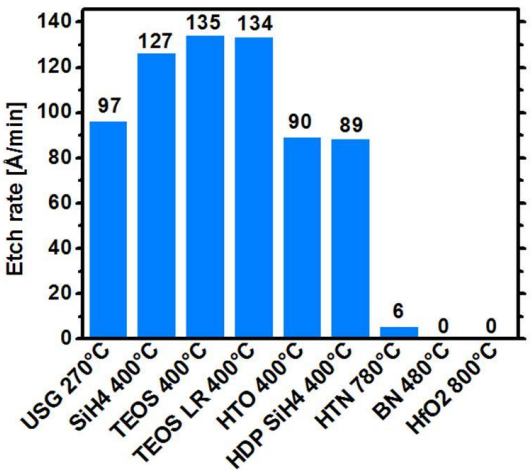


Figure III.3.5: Etch rate measured on sacrificial and etch-stop layers. Oxides and HTN were exposed 10min under vapor HF. BN and HfO_2 were respectively measured after an exposition of 80min and 2h.

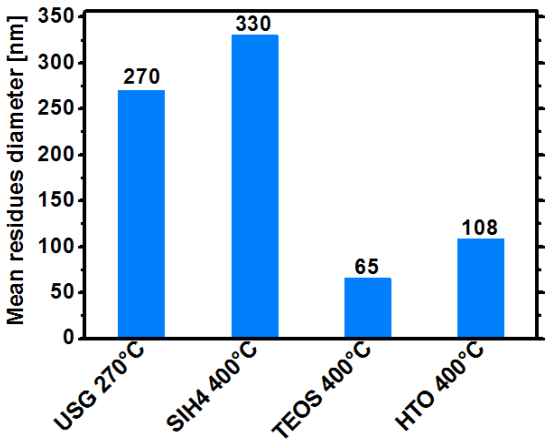
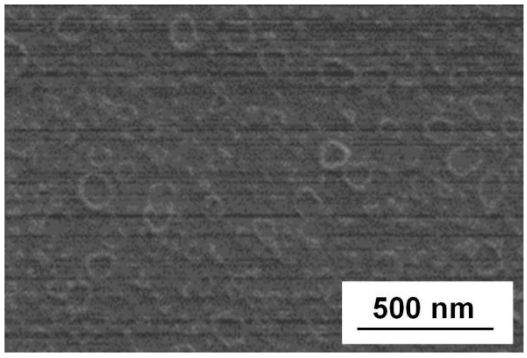
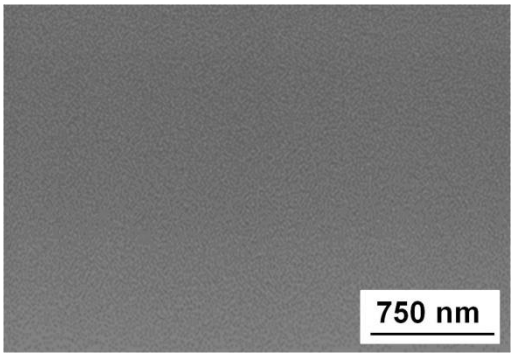


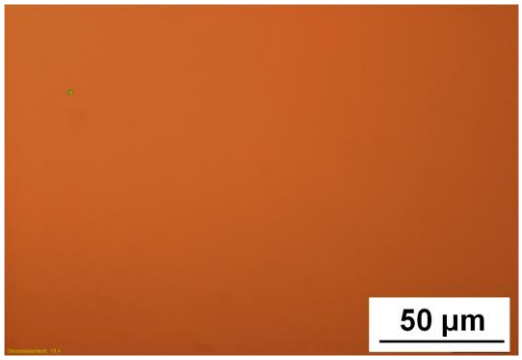
Figure III.3.6: Mean residues diameter after 10min vapor HF exposition for some oxides. The other materials (TEOS LR, HDP SiH_4, HTN, HfO_2 and BN) did not let any residues after the etching process.



(a)



(b)



(c)

Figure III.3.7: SEM (a-b) and optical (c) micrographs of etch-stop layer after vapor HF exposition: (a),(b) and (c) correspond respectively to a HTN after 10min of exposition with a high presence of crater, an amorphous BN layer after 80min of exposition with a very clean surface and a crystalline HfO_2 annealed at 800°C for 3min after 2h of exposition with a clean surface too.

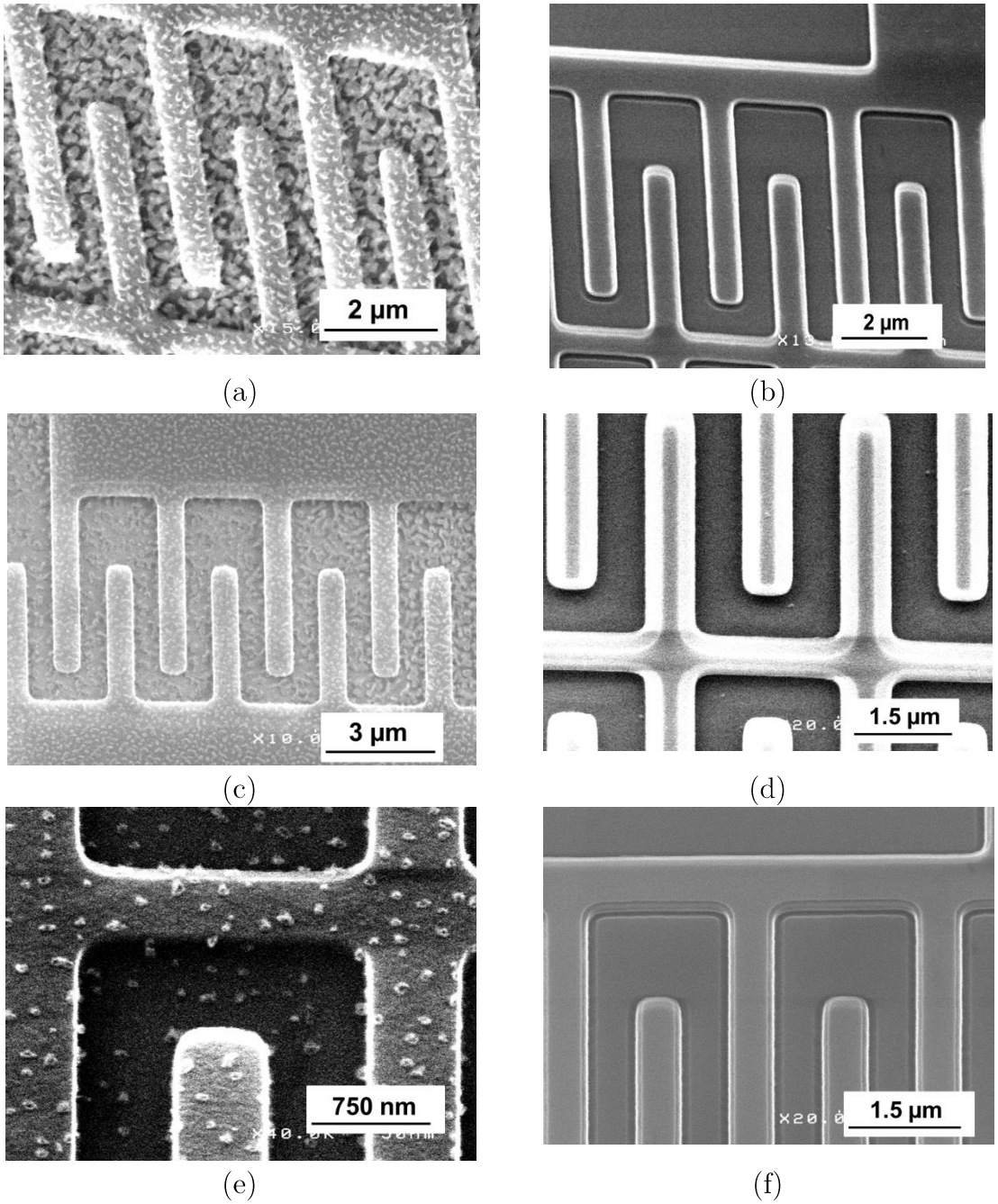
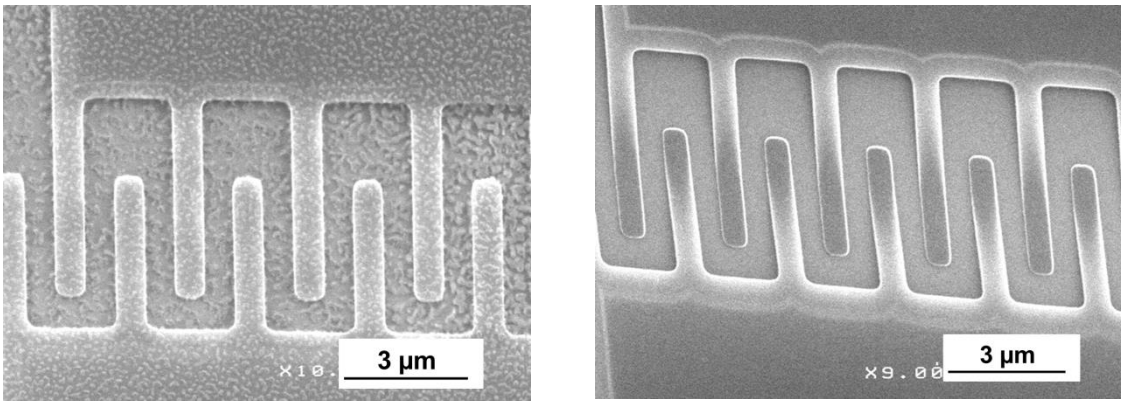


Figure III.3.8: SEM micrographs of a silicon structure sandwiched into different kind of sacrificial layers (a) a SiH_4; (b) a TEOS LR; (c) a USG; (d) a TEOS; (e) a HTO; (f) a HDP SiH_4. (a), (c) and (e) show a high presence of residues after 10min of exposition unlike (b), (d) and (f). These residues can damage the beam and can make it not functional.



(a) (b)

Figure III.3.9: SEM micrographs of a silicon structure sandwiched into a USG sacrificial layer etched 10min under vapor HF environment before (a) and after (b) water rinsing step and oven drying.

This study presented some results about etch rates and residual dimensions on vapor HF etching of materials used for NEMS processing. It is shown that USG and SiH_4, usually used in back-end processes, are not suitable for the vapor HF release contrary to TEOS, TEOS LR and HDP SiH_4. These oxides do not let any residues after vapor HF exposition. Furthermore BN shows a remarkable resistance property and constitutes a good etch-stop layer for vapor HF etching process. The latter can be deposited with a very low thickness suitable for the above-IC integration, for example between 20 and 60nm.

III.2 NEMS-back-end interconnection

This study consists in ensuring a good electrical contact between NEMS and CMOS. In practice, the related technological steps occur after NEMS patterning and just before the release process, as described in section II.2. It is first important to take a look at the depth of these vias, as illustrated in Figure III.3.10. During CMOS substrate preparation, the first step was to fill in the back-end apertures with a TiN barrier and Cu. The main idea was to raise the last metal level of the back-end in order to make easier the interconnection step (h_1 via). Indeed, as depicted in Figure III.3.10, this strategy allows a reduction of 1.7µm of via depth. Besides it is interesting to investigate the possibility to contact directly the sensing part with the metal back-end without Cu pre-filling (h_2 via) to make 3D above-IC integration strategy more flexible with respect to the CMOS technology. Considering the stack thickness, it is possible to evaluate the vias depth to fill: h_1 is about 1.4µm and h_2 around 3.1µm. In order to get a high density of resonators, vias diameter ϕ must be as thin as possible.

Consequently, the metal used for this purpose must fulfill some criteria. Firstly, its deposition temperature must not exceed 450°C. Secondly, it has to be inert under vapor HF exposition. Thirdly, it must ensure the contact between c-Si layer and back-end with a low contact resistance.

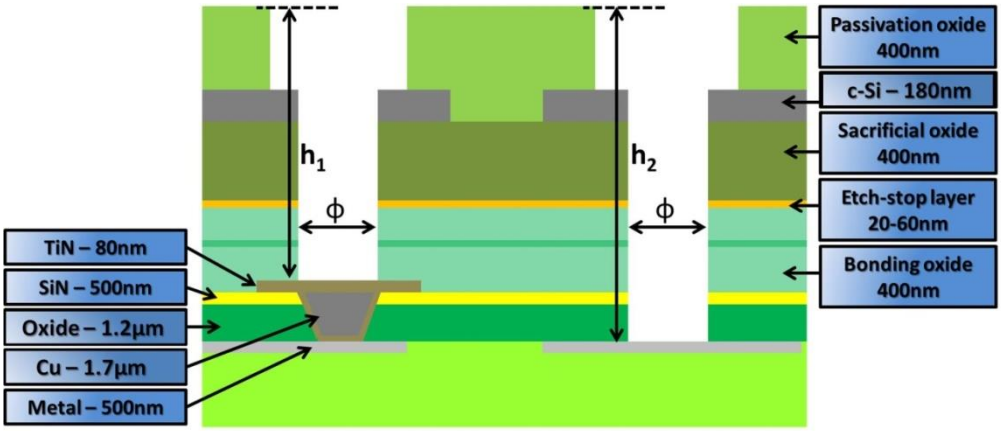


Figure III.3.10: Cross-sectional schematic of the vias fabrication. h_1 and h_2 respectively correspond to the interconnection depth between c-Si and TiN barrier, and between c-Si and the last back-end metal level. ϕ represents the via diameter.

Table III.5 presents some metallic materials compatible with those requirements. This table reports the growth method and the reactivity with vapor HF. Even with a lower temperature than the maximum thermal budget limit, Ni and Cu are excluded because of their reactivity with HF. Besides, a conformal material (defined in section III.2.2) is required for a good electrical contact between back-end and c-Si. A CVD deposited material is suitable. According to Table III.5, tungsten silicide (WSi) could be a good candidate. Furthermore, this material shows low contact resistance with silicon as studied in [Ohb87]. However, its behavior under vapor HF is not known and has to be investigated. Next sections will report on some results about WSi performance.

Material	Growth method and Temperature (°C)	Reaction with vapor HF
AlCu	PVD / T<450°C	No
AlSi	PVD/~175°C	No
W	PVD/~300°C	No
WSi	CVD/~300°C	?
TiN	PVD/~350°C or CVD/~400°C	No
Ti	PVD/<350°C	No
Cu	PVD/~30°C or CVD/~200°C or ECD/~25°C	Yes
Ni	PVD/~20°C or ECD/~55°C	Yes

Table III.5: Characteristics of various metals for interconnection purposes.

III.2.1 –HF resistance evaluation

For this study, two substrates were prepared as illustrated in Figure III.3.11. On these substrates, a first thermal oxidation was performed to form a 500nm thick oxide. The presence of this oxide allows a study of the metal permeability. A 100nm thick Ti-TiN barrier is deposited on one wafer followed by a 250nm WSi deposition on all wafers. Ti-TiN is generally deposited to improve the adherence of WSi during via filling and must be studied as well.

Several exposition durations were imposed for this study: 30min, 1h and 1h20min. The different samples were characterized by SEM cross-section. The results are presented in Figure III.3.12. Even for a 1h20 exposition, WSi seems almost intact. The different values of WSi thickness are linked to its surface topography, as illustrated in the tilted view of Figure III.3.13. Furthermore, the silicon oxide thickness does not change after HF exposition. According to these results, WSi and WSi-TiTiN stacks do not react and are impermeable to vapor HF.

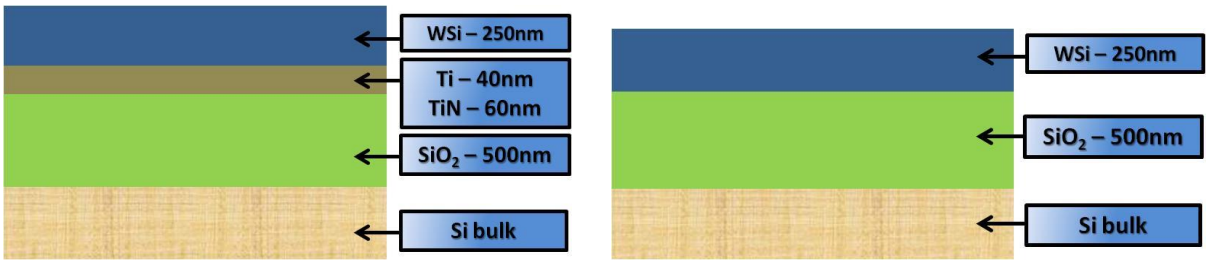
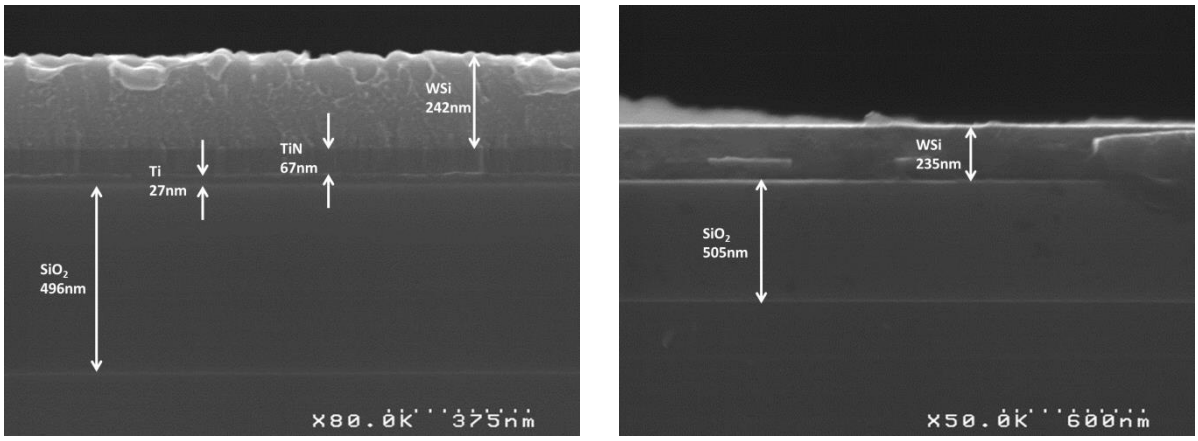
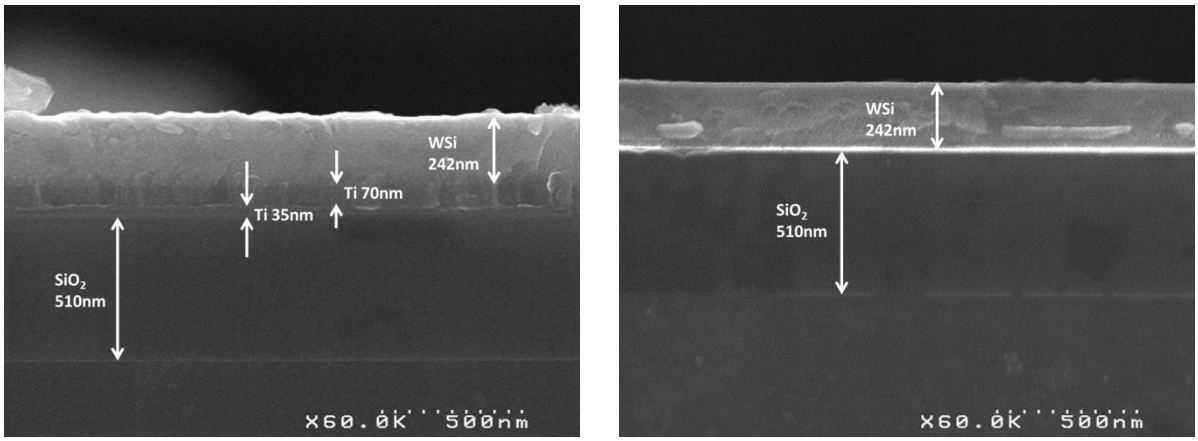


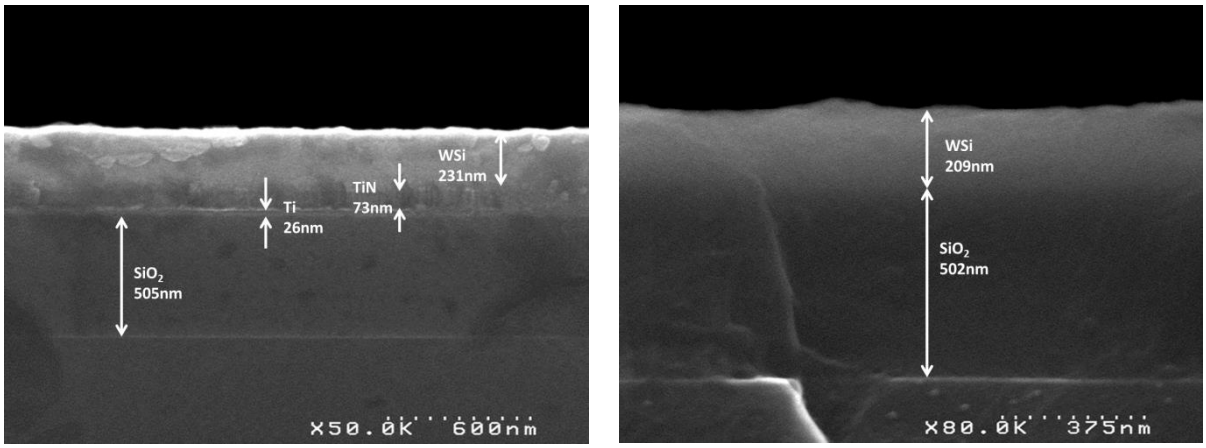
Figure III.3.11: Cross-section of the wafers used for vapor HF resistance test.



Before exposition

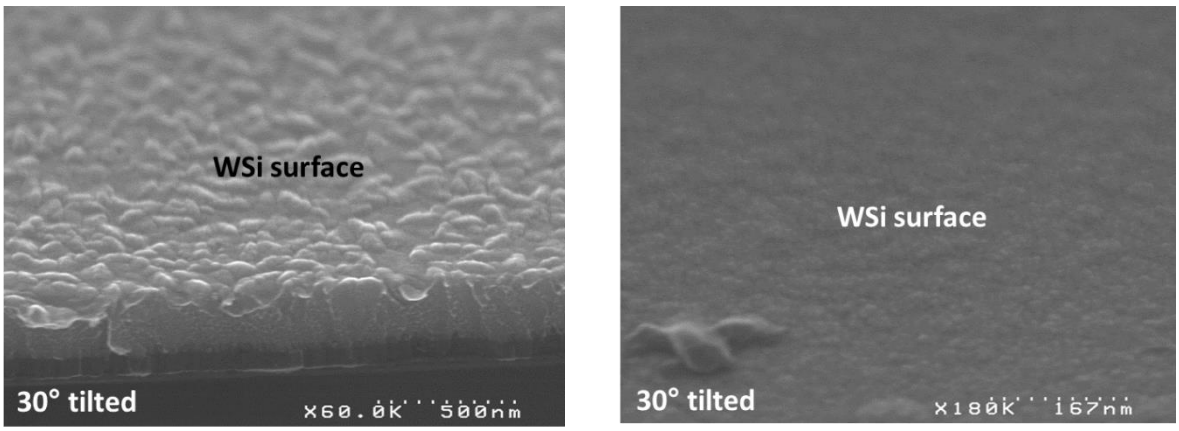


After 30min of exposition

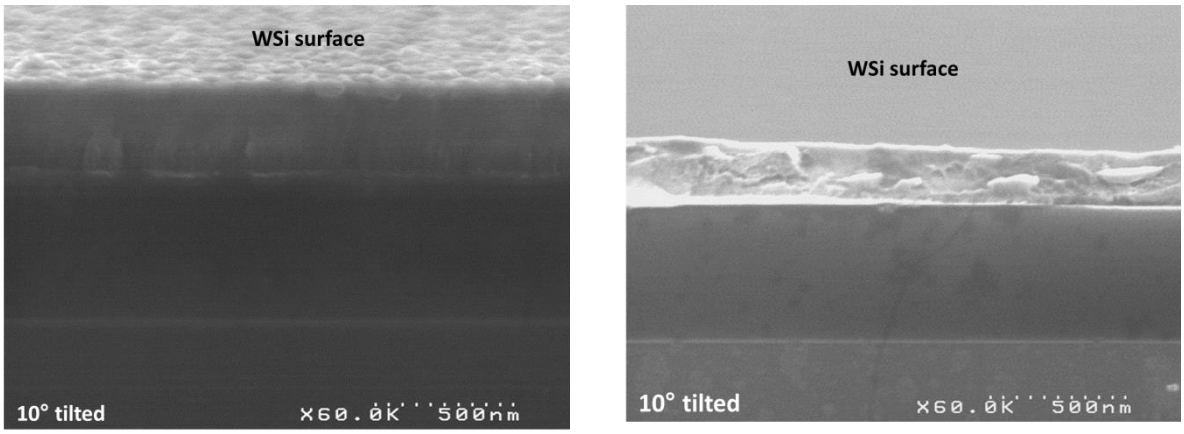


After 1h20 of exposition

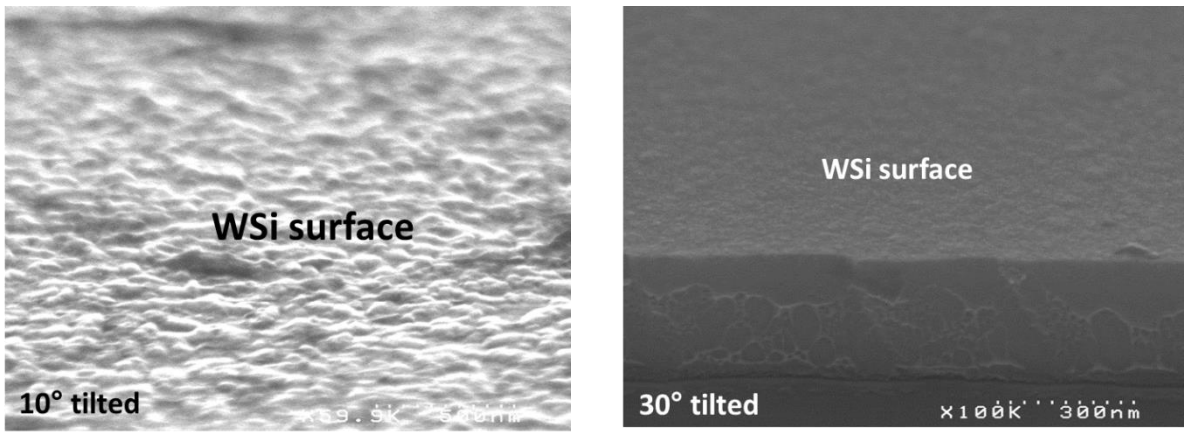
Figure III.3.12: Cross-sectional SEM view of WSi-TiTiN-SiO_2 and WSi-SiO_2 after exposition under vapor HF.



Before exposition



After 1h of exposition



After 1h20 of exposition

Figure III.3.13: Cross-sectional tilted SEM view after vapor HF exposition.

III.2.2 –Conformity evaluation

This section deals with the conformal behavior of metals for via filling. A material is conformal if its thickness is the same on each part of a via (bottom part, wall) after its deposition. A CVD material will be more conformal than a PVD material, making WSi optimal respect to standard metal used for NEMS metallization, such as aluminum-silicon (AlSi) or aluminum-copper (AlCu) alloys deposited by PVD. In this study, the conformal character of WSi is investigated and compared with AlSi's one.

Figure III.3.14 depicts the experimental protocol. Silicon dioxide is deposited on silicon substrate with different thicknesses corresponding to h_1 and h_2 (see section III.2). This dielectric layer simulates the stack present between c-Si and metal back-end layers, as described in Figure III.3.10. The oxide is then patterned with different diameters ϕ. After that, a metal deposition is performed. Three different depositions are performed: one with 3.2µm and 4.8µm thick AlSi respectively for 1.5µm and 3.2µm thick oxide; another with a stack {Ti (40nm), TiN (60nm), WSi (220nm)}, and a last one with a 220nm thick WSi. The conformity of each material is studied with Focused Ion Beam (FIB) and SEM observations. Some micrographs are depicted in Figures III.3.15, III.3.16 and III.3.17 with dimensional measurements on Table III.6, III.7 and III.8. The presence of tungsten comes from FIB operation.

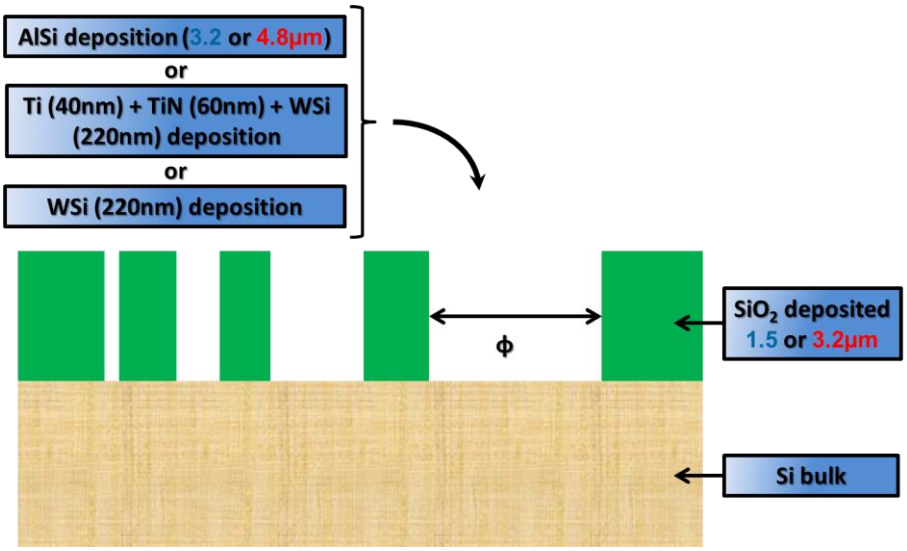
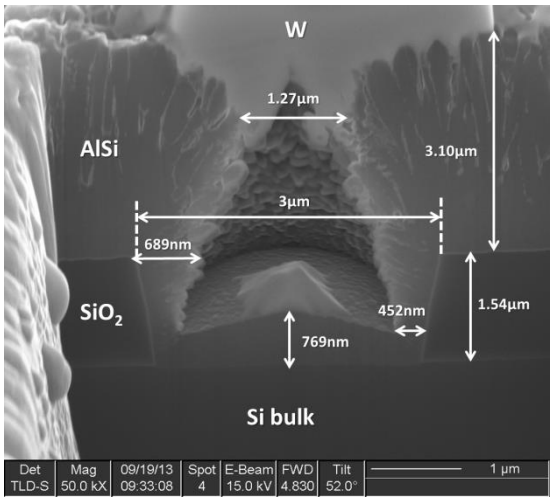
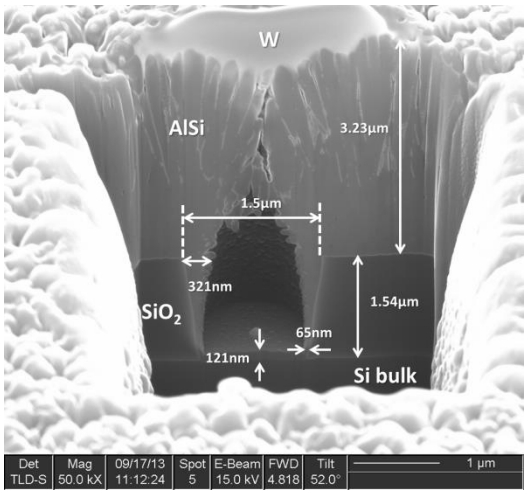


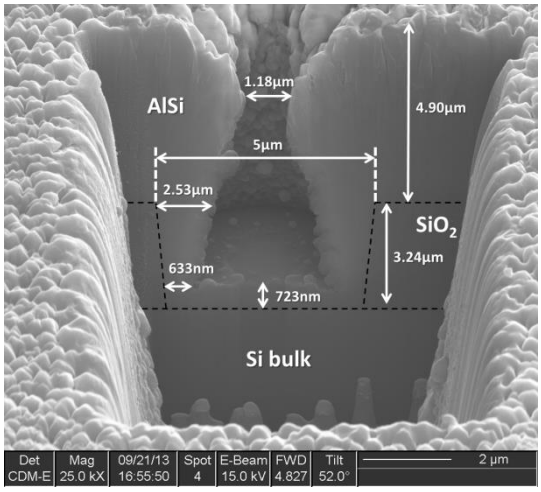
Figure III.3.14: Schematic description of via filling experiment.



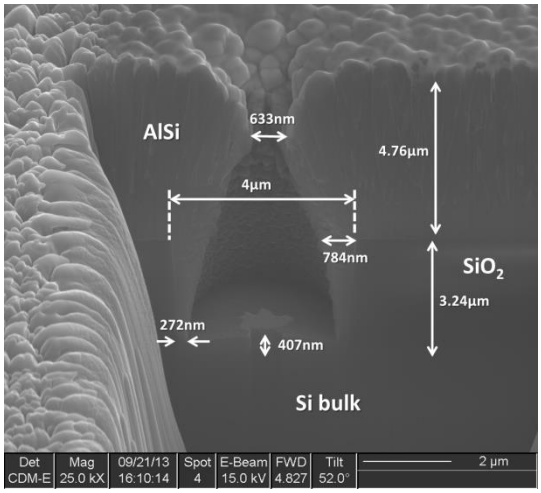
AlSi via filling with a 3µm diameter and a 1.54µm height.



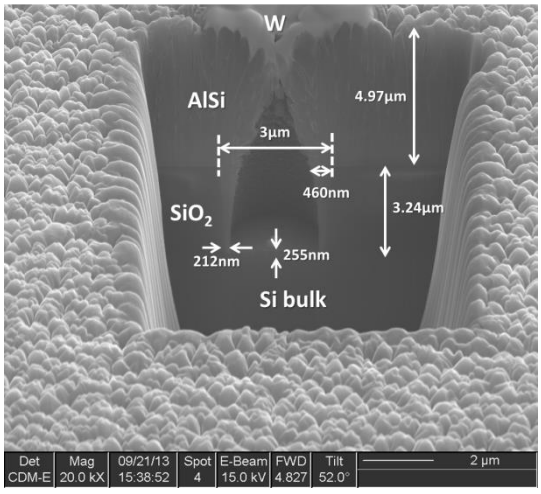
AlSi via filling with a 1.5µm diameter and a 1.54µm height.



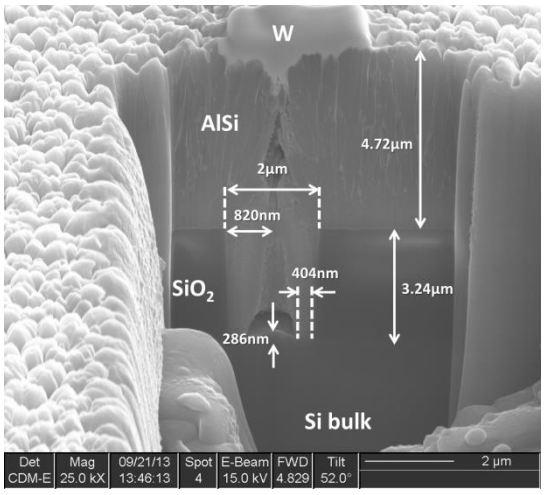
AlSi via filling with a 5µm diameter and a 3.24µm height.



AlSi via filling with a 4µm diameter and a 3.24µm height.

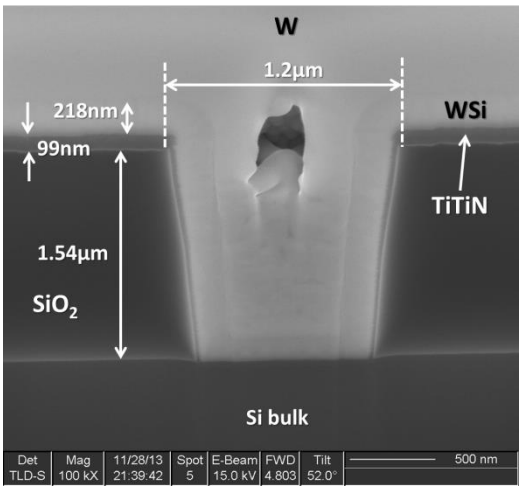


AlSi via filling with a 3µm diameter and a 3.24µm height.

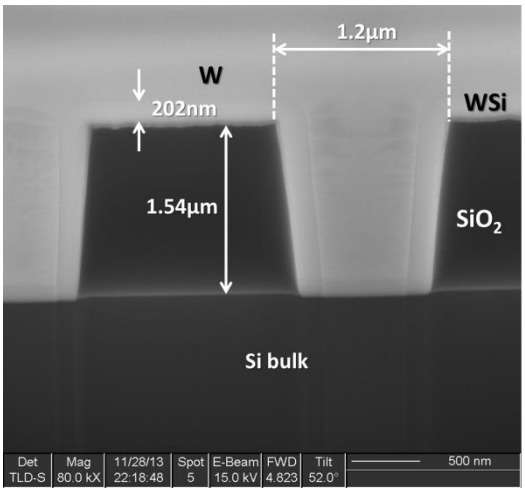


AlSi via filling with a 2µm diameter and a 3.24µm height.

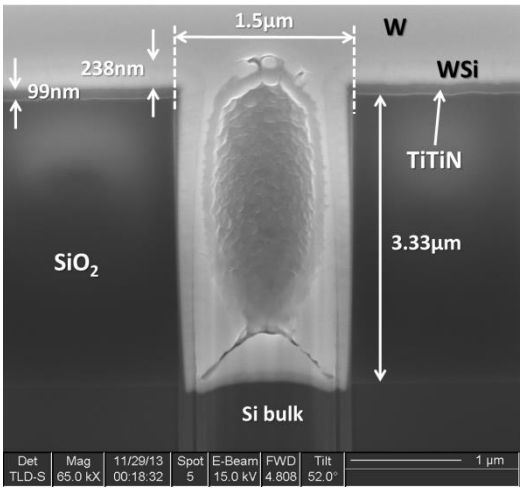
Figure III.3.15: SEM micrographs of vias filling with different aspect ratio using AlSi.



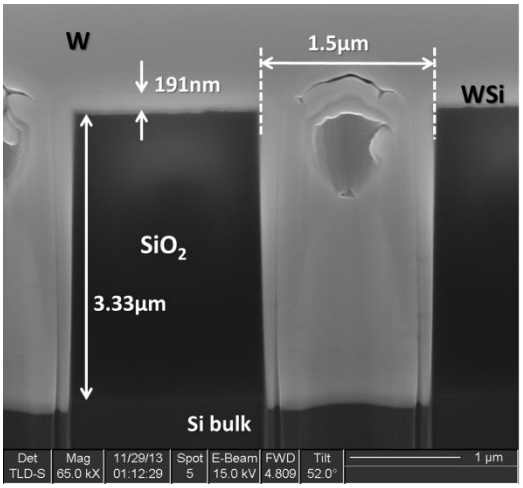
Ti-TiN and WSi via filling with a 1.2µm diameter and a 1.54µm height.



WSi via filling with a 1.2µm diameter and a 1.54µm height.



Ti-TiN and WSi via filling with a 1.54µm diameter and a 3.33µm height.



WSi via filling with a 1.54µm diameter and a 3.33µm height.

Figure III.3.16: SEM micrographs of vias filling with different aspect ratio using Ti-TiN and WSi.

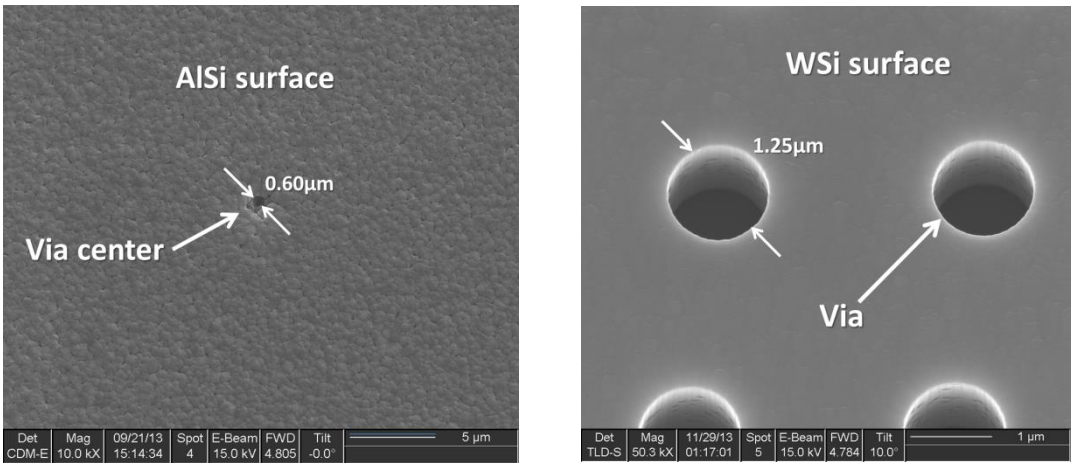


Figure III.3.17: SEM micrographs top view of substrate surfaces after metal deposition. On the left and on the right are respectively depicted a surface around a 3µm diameter via after a 3.2µm AlSi deposition and a 1.5µm diameter via after a 220nm WSi deposition.

All these results show that AlSi, generally used as NEMS interconnection [Mar13], is on the one hand not a conformal material and on the other hand not convenient for the electrical connection between the sensing and the back-end parts. Indeed, Table III.6 shows that the thicknesses present on the top (*i.e.z*), the base (*i.e. y*) and the bottom (*i.e.x*) part of the via (see Figure III.3.18) do not exceed a quarter of the layer located on the oxide (*u*). These results are obtained with an initial thickness deposition of material: 3.2µm and 4.8µm respectively for 1.5µm and 3.2µm via height. WSi and Ti-TiN – WSi materials show better results. The thickness ratio present at each part of the vias (*x*, *y* and *z*) respect to the one present on the oxide (*u*) is higher than 40%, reaching sometimes more than 80%, with an initial thickness deposition of 100nm for Ti-TiN barrier and 220nm for WSi. A thicker deposition is not necessary to ensure the continuity of the contact for WSi with respect to AlSi. These results strengthen the idea to use WSi as interconnection metal for 3D NEMS-CMOS co-integration.

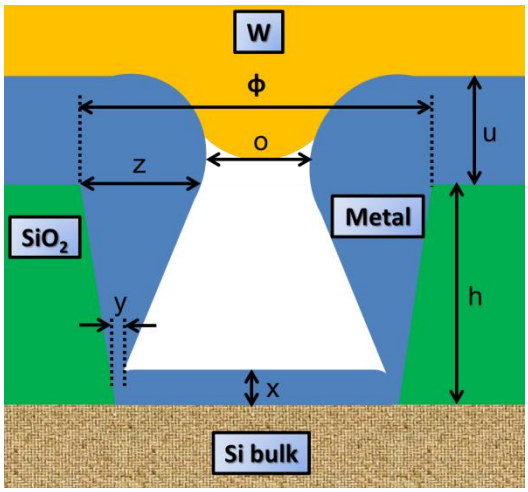


Figure III.3.18: Schematic representation of via filling after FIB.

ϕ (µm)	h (µm)	x (nm)	y (nm)	z (nm)	o (nm)	u (µm)	x/u	y/u	z/u
1.5	1.54	121	65	321	0	3.23	**4%**	**2%**	**10%**
2	1.54	309	177	574	155	3.10	**10%**	**6%**	**19%**
3	1.54	769	452	689	1270	3.10	**25%**	**15%**	**22%**
2	3.24	286	404	820	0	4.72	**6%**	**9%**	**17%**
2.5	3.24	306	341	956	0	4.76	**6%**	**7%**	**20%**
3	3.24	255	212	537	0	4.97	**5%**	**4%**	**11%**
4	3.24	407	272	784	633	4.76	**9%**	**6%**	**16%**
4.5	3.24	527	410	1347	1405	4.82	**11%**	**9%**	**28%**
5	3.24	723	633	2531	1175	4.90	**15%**	**13%**	**52%**

Table III.6: Results of via filling with AlSi

ϕ (µm)	h (µm)	x (nm)	y (nm)	z (nm)	o (µm)	u (nm)	x/u	y/u	z/u
1.2	1.54	30	30	30	1.26	100	**30%**	**30%**	**30%**
1.2	3.2	35	44	44	1.20	99	**35%**	**44%**	**44%**

Table III.7: Results of via filling with Ti-TiN.

ϕ (µm)	h (µm)	x (nm)	y (nm)	z (nm)	o (µm)	u (nm)	x/u	y/u	z/u
1.2 [a]	1.54	166	187	218	0.83	218	**76%**	**86%**	**100%**
1.2 [b]	1.54	160	167	191	0.83	210	**76%**	**80%**	**91%**
1.5 [a]	3.33	110	108	183	1.16	241	**46%**	**45%**	**76%**
1.5 [b]	3.33	110	104	191	1.20	191	**58%**	**54%**	**100%**

Table III.8: Results of via filling with WSi ([a] with Ti-TiN barrier; [b] without Ti-TiN).

III.3 Molecular bonding

This section will focus on the first step of the assembly: the molecular bonding between CMOS and SOI substrates (see II.2.3).This part will describe the most important related requirements.

III.3.1 – CMOS substrate characteristics

For this study, substrates comprising only the last metal level of an AMS 0.35µm technology were used for the first bonding trials. Front-end and first metal levels of back-end were not necessary as they only induce a weak topography with respect to the dielectric apertures above the last metal level.

These back-end substrates are composed of an elementary die repeated on all the substrate as described in Figure III.2.14. It is important first to analyze the main patterns and topography induced on the surface. Figure III.3.19 depicts a global view of the test-vehicle chip from a layout point of view, with some optical microscope views on specific areas. Insets present in Figure III.2.19-a show apertures through the dielectrics back-end down to the last metal level with various dimensions: from 2-3.5µm (in *i*; *v* and *vi*) to 90 – 100µm (in *ii; iii; iv*). These apertures can be surrounded by many of other one (like in *i*; *vi*; *v* on the top) or not (*ii*; *iii*; *iv* and *v* on the bottom). Their density may be crucial for the planarization of copper and bonding oxide: they create a "dummies effect" (like in microelectronics) which attenuates the dishing effect (see Figure III.3.20) after CMP and so the topography. Dishing corresponds to the difference of height between oxide and copper obtained after CMP. Since this density is not the same everywhere on the chip, a careful control of the planarity is necessary, specifically in the areas with low density and large apertures (illustrated on Figure III.3.20) [Par02-Ngu00-Fay00].

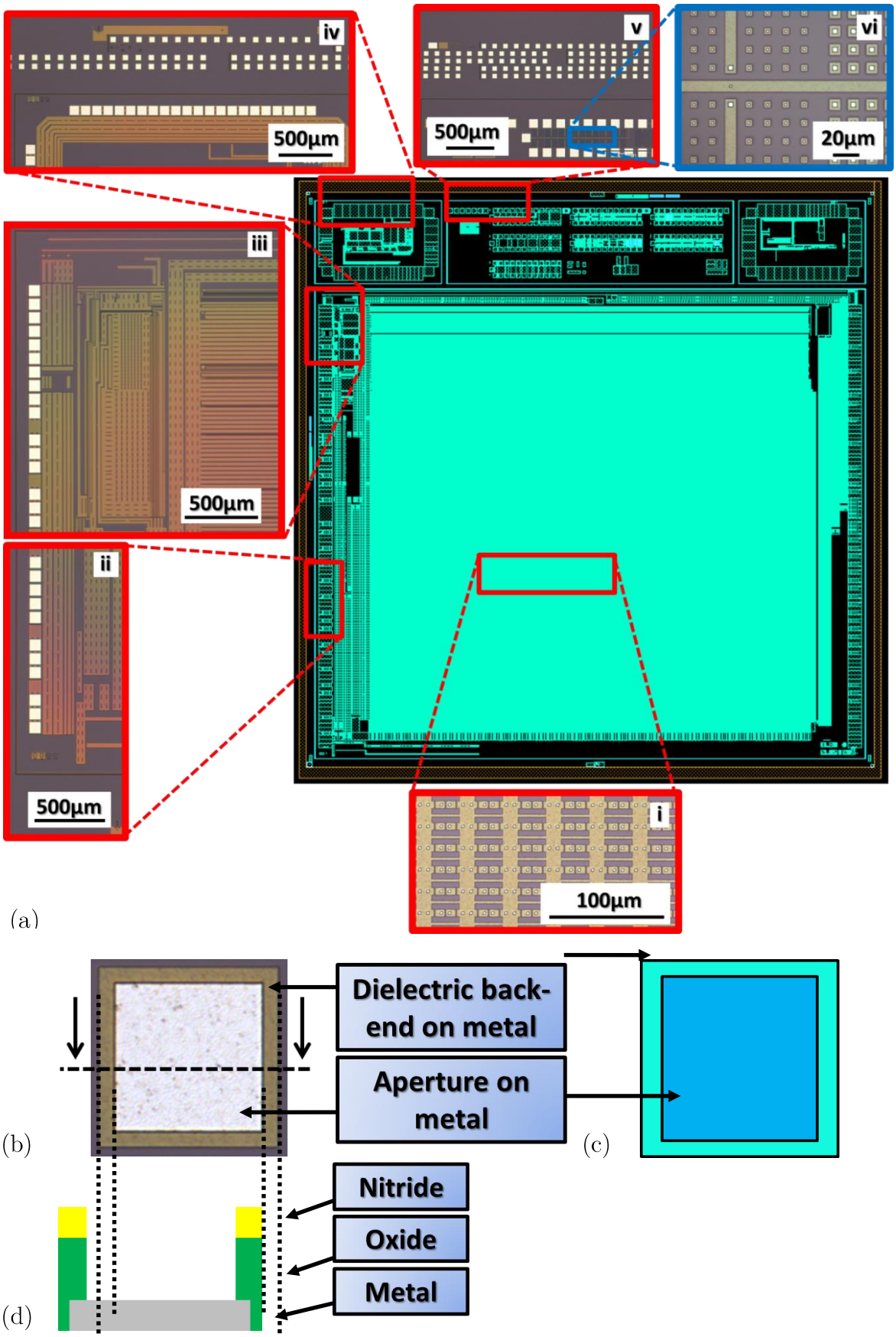


Figure III.3.19: Chip layout representation with optical view of typical zones in insets (a); Description of optical view contents (b) with correspondence in layout (c) and cross section schematic (d).

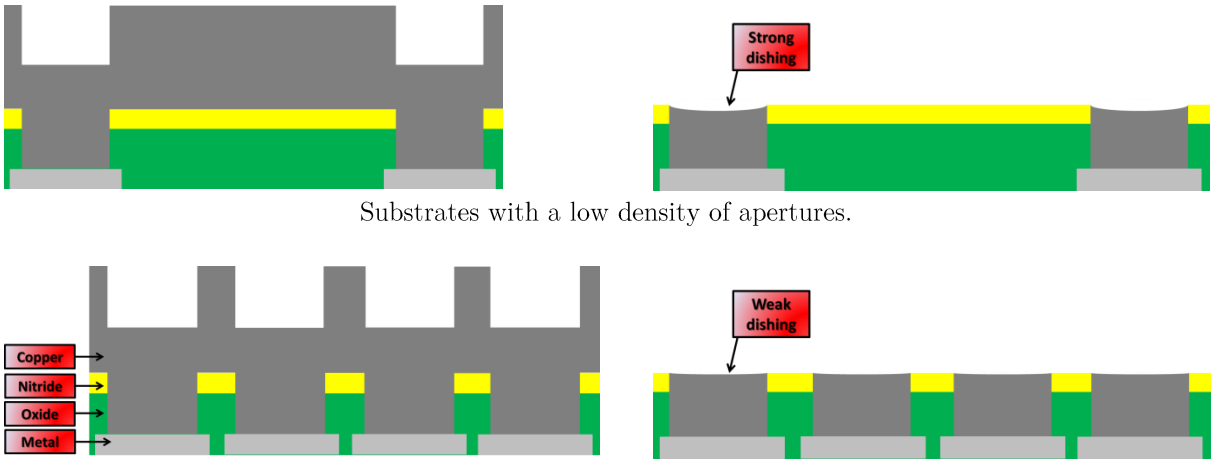


Figure III.3.20: Before (on the left) and after (on the right) Cu CMP and illustration of the apertures density effect.

III.3.2 – Results after grinding

After preparation as described in Figure III.2.12, these substrates were bonded on SOI wafers prepared following the process flow presented in section II.2.1 with TEOS LR as sacrificial layer. BN and HfO_2 were deposited as etch-stop layer followed by a thermal annealing respectively at 600°C for 1h for BN outgassing and 750°C for 3min for HfO_2 crystallization. After direct bonding, a rough polishing is performed. The results of these polishing steps are depicted in Figure III.3.21. Grey parts correspond to silicon bulk of the SOI wafer. These photographs show that some parts have been delaminated during the grinding. In these particular areas, the CMOS wafer patterns are visible. This delamination may be dangerous for the substrates during the following process flow, particularly during the etching steps of silicon bulk and BOX of SOI substrate. It is important to precisely localize the weakness points of the stack on which the delamination occurred in order to understand their origin.

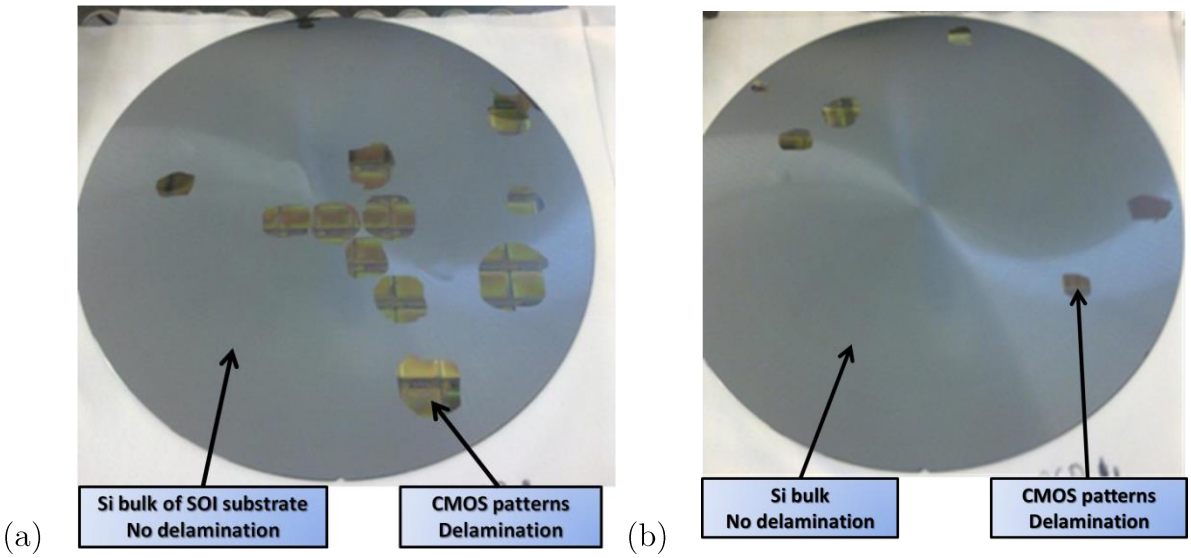
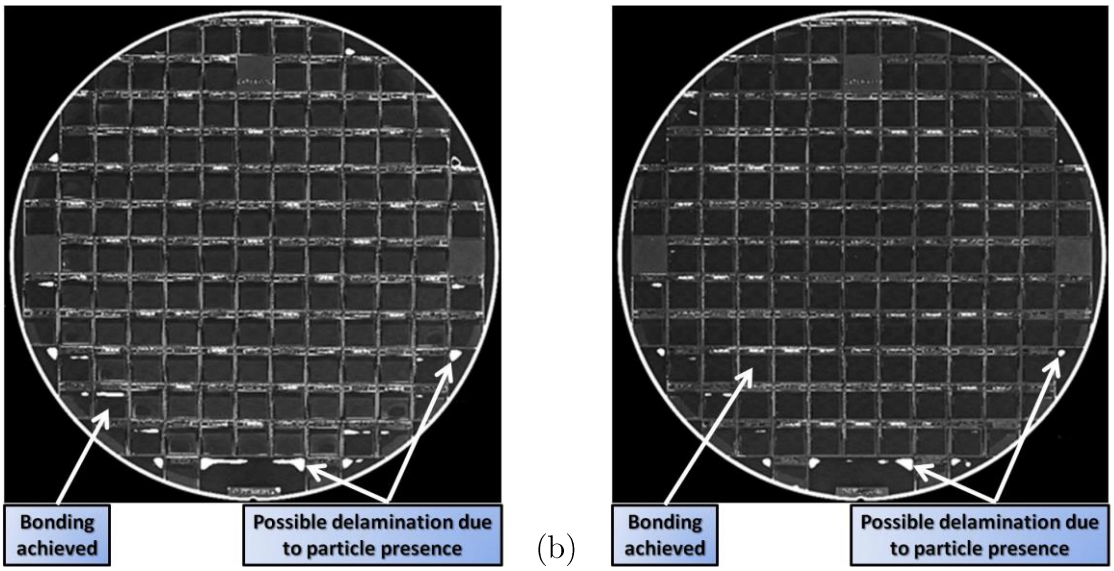


Figure III.3.21: Photographs of substrates with BN (a) and HfO_2 (b) as etch-stop layer after rough polishing.

III.3.3 – SAM analysis

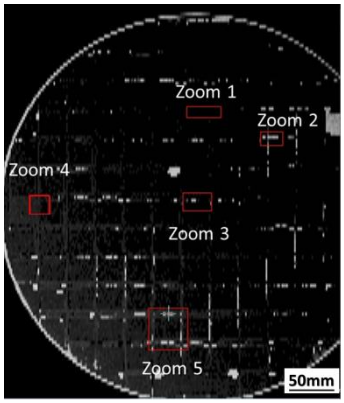
As described in section II.2.11, SAM method is a common technique for bonding analysis. Figure III.3.22 depicts acoustic photographs of substrates presented above, with a focus on particular zones (Figure III.3.23). These characterizations were performed just after the molecular bonding step. Black areas mean that no acoustic reflection occurs and thus indicate a complete bonding, whereas white zones show that the bonding between the surfaces did not happen for two possible reasons: particles presence and surface topography problem. As different kinds of material are present on the sample, the acoustic impedance difference (particularly between metals and oxides, see Table III.1) may induce some reflections of the acoustic waves which can be at the origin of grey and white zones. A comparison between several chips inside a same wafer and also in-between several wafers must be performed on problematic zones. The machine used here has a lateral resolution of almost 10µm, which means that patterns smaller than 10µm cannot be observed with acoustic microscopy.

The different zooms depicted on Figure III.3.23 show no-bonded areas, probably due to a topography problem. According to Figure III.3.19, these zones correspond to the apertures filled by copper and polished just after. Therefore, a careful topography control has to be performed in these sites.

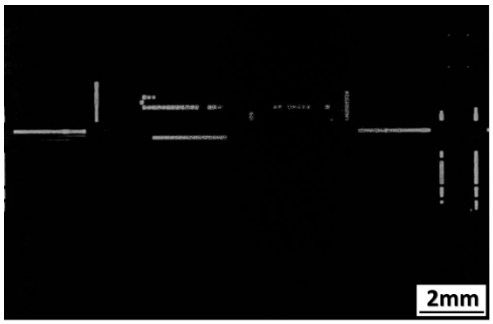


(a) (b)

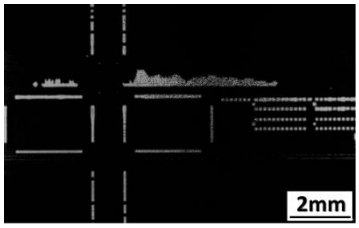
Figure III.2.22: SAM micrographs of wafers after bonding



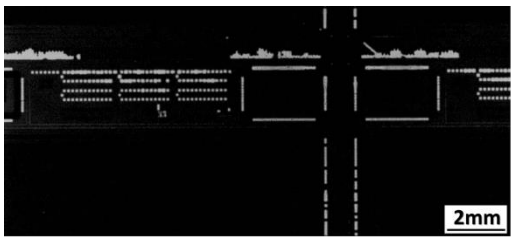
(a) Global view of wafer via acoustic microscopy.



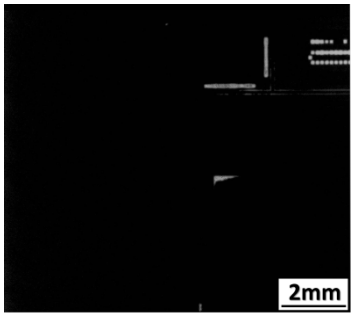
(b) Zoom 1 micrograph.



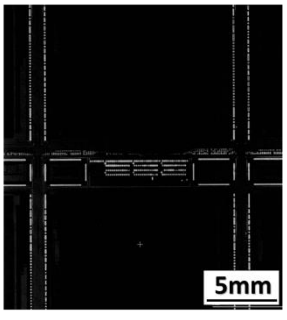
(c) Zoom 2 micrograph.



(d) Zoom 3 micrograph.



(e) Zoom 4 micrograph.



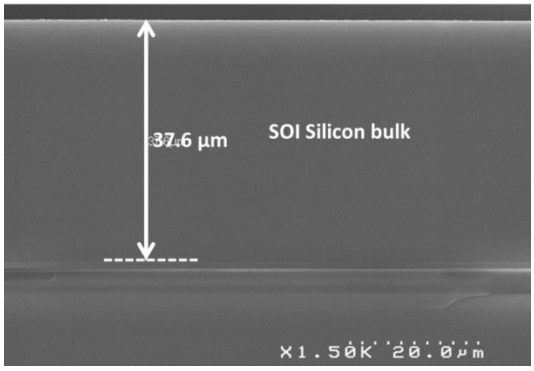
(f) Zoom 5 micrograph.

Figure III.3.23: SAM analysis on particular zones.

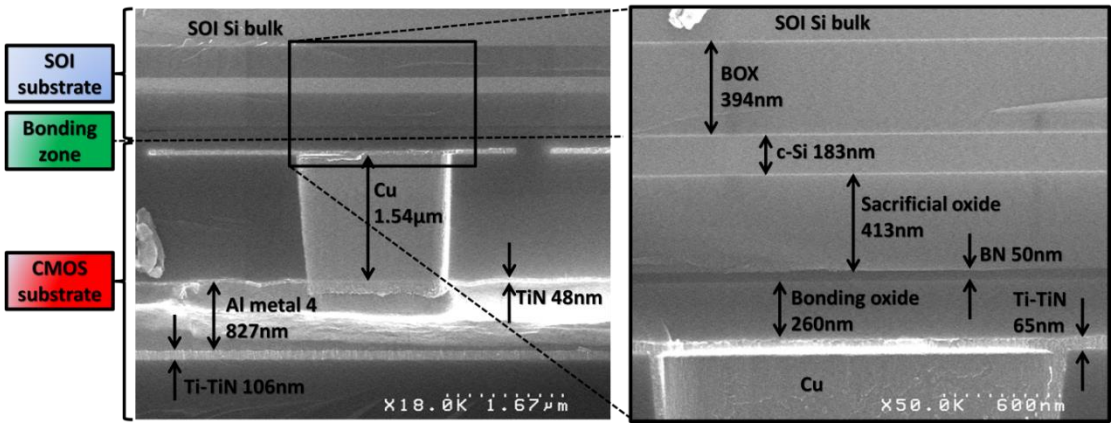
III.3.4 – SEM analysis

Acoustic microscopy allowed determining the zones where the substrates are not bonded. Nevertheless, these photographs are not sufficient to analyze the precise origin of delamination. Even if the microscope vertical resolution is around 10nm, the uncertainty on the different layers thicknesses of the stack is still important, particularly concerning the SOI silicon bulk part after rough polishing. Cross-sectional SEM analysis is thus necessary. These micrographs are shown on Figure III.3.24, III.3.25 and III.3.26.

The first figure illustrates a successful direct bonding. The bonding interface between TEOS material from each substrate is not visible. A delamination case is depicted on Figure III.3.25. This bonding problem is detected since the focal planes of the different substrates are different. Furthermore, it shows that delamination occurs between etch-stop layer (here BN) and bonding oxide. This is confirmed by Figure III.3.26, III.3.27 and III.3.28 where the surface of bonding oxide is visible (III.3.25 and 26) and the underlying surface of BN (III.3.27). Several hypotheses may explain this bonding failure after grinding, such as surface problem like topography, particles presence (as illustrated on Figure III.3.29) or interface problem like adherence between the etch-stop layer and the bonding oxide.



General view of SOI substrate bonded on CMOS wafer.



Zoom views near the bonding zone.

Figure III.3.24: Cross-sectional SEM micrographs of SOI and CMOS substrates assembled by direct bonding.

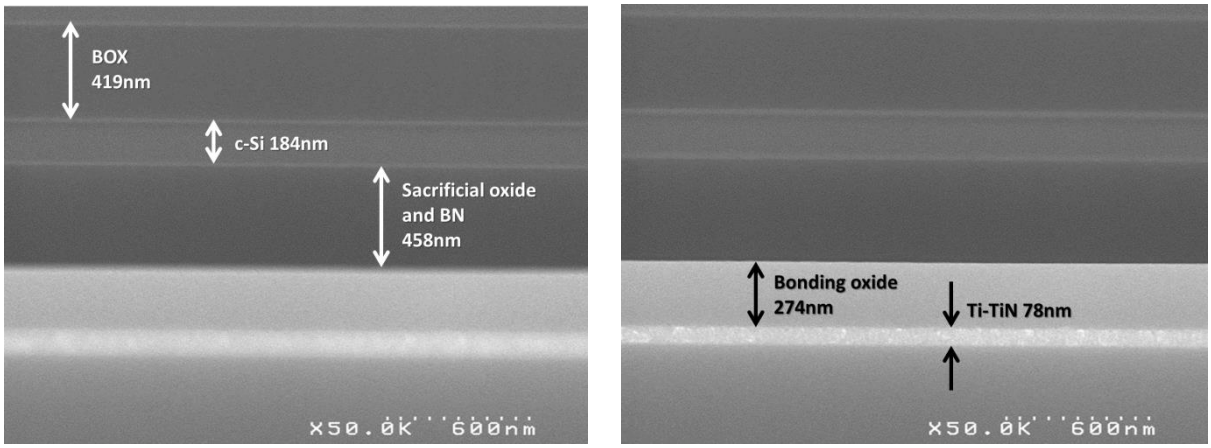


Figure III.3.25: Cross-sectional SEM micrographs on delamination zone with a focus on SOI (on the left) and on CMOS substrate (on the right).

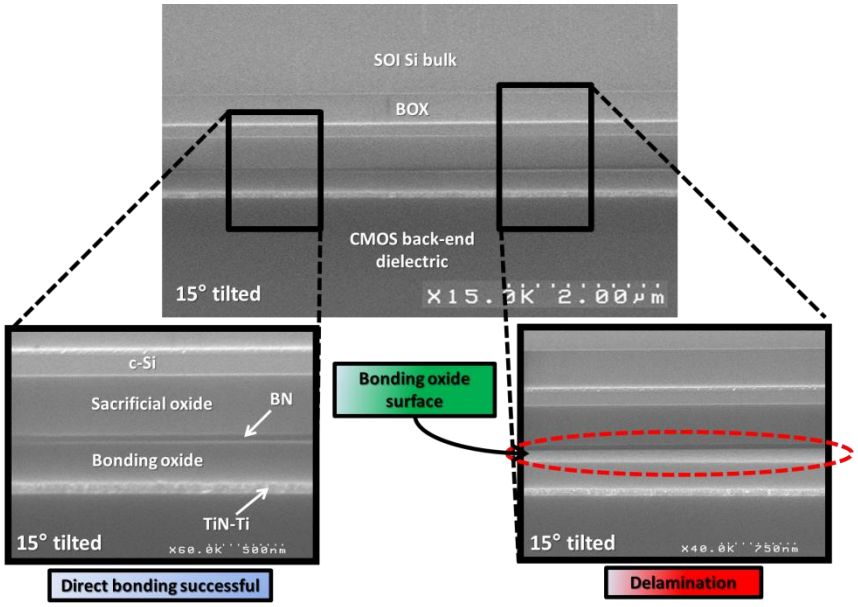


Figure III.3.26: Cross-sectional SEM micrographs on direct bonding zones (on the left) and delamination (on the right) zones.

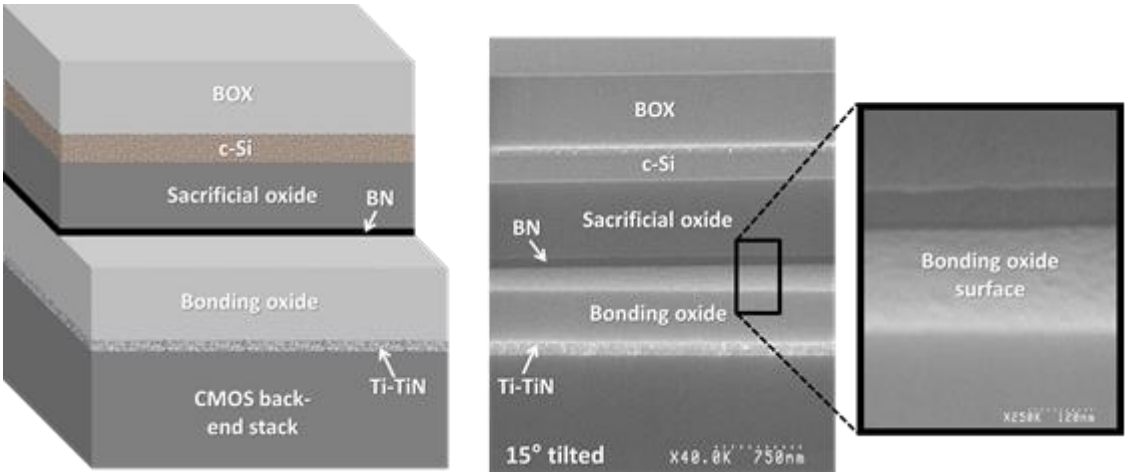
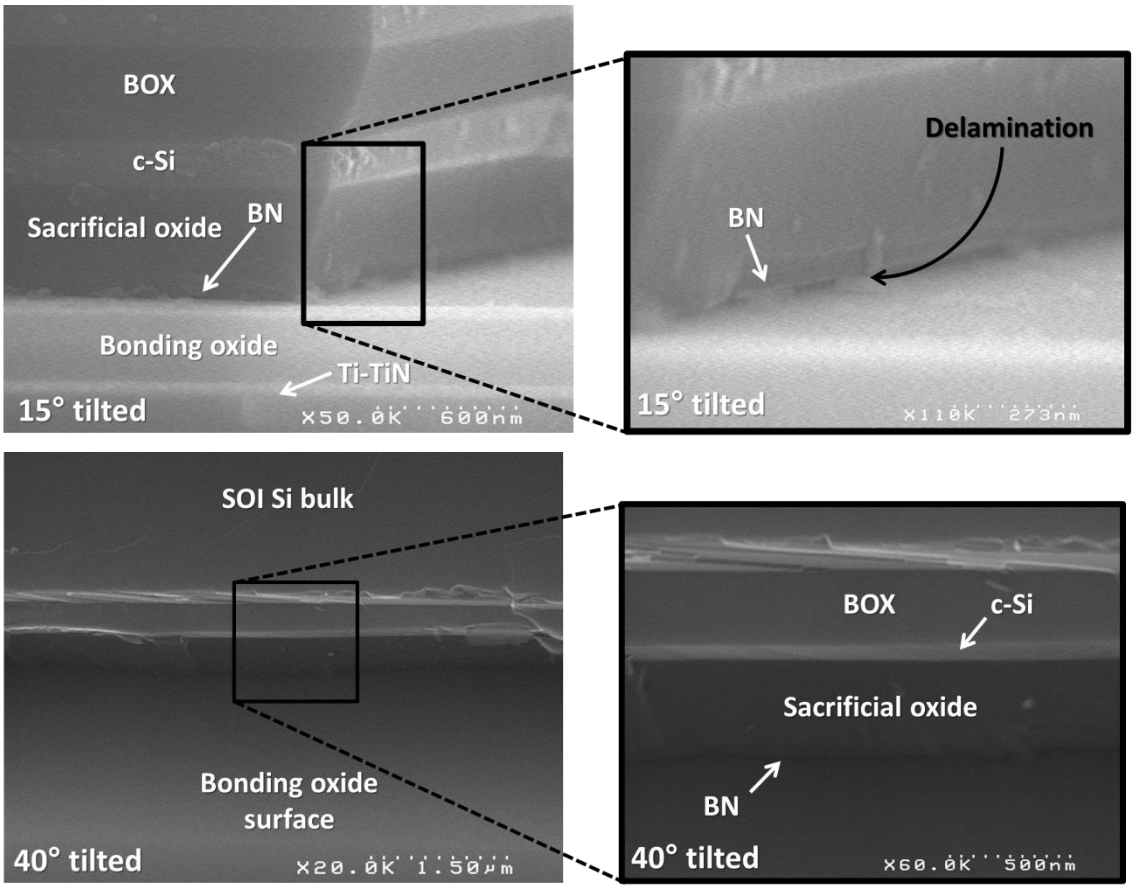
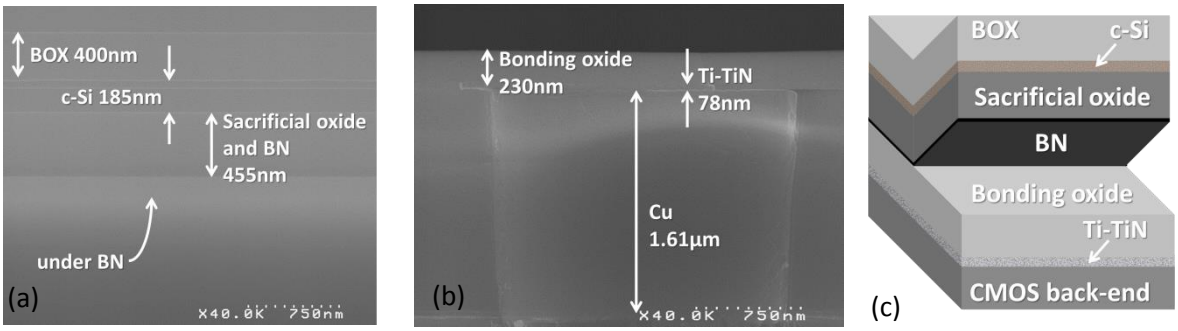


Figure III.3.27: Schematic representation (on the left) and cross-sectional SEM micrographs (on the right) of the delamination.



Zoom on SOI substrates.



Zoom on SOI (a) and CMOS (b) substrates with explanation schematic of delamination (c).

Figure III.3.28: Cross-sectional SEM micrographs of delamination for different areas.

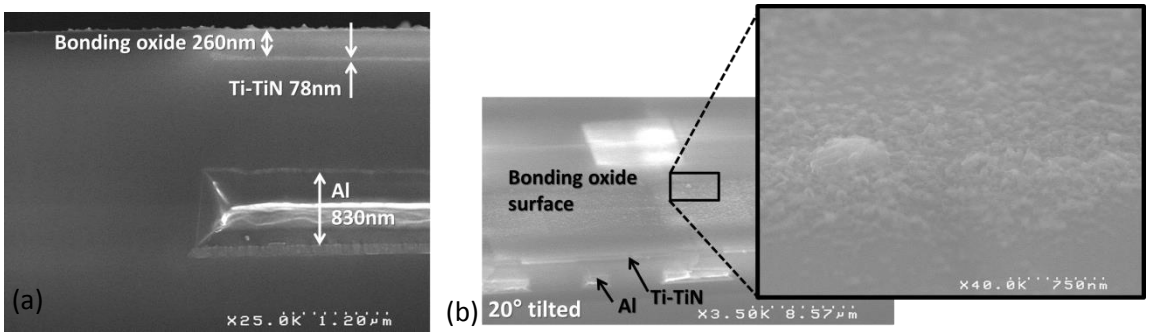


Figure III.3.29: SEM micrographs of CMOS substrates with different possible origins for delamination: planarity problem (a) and particles presence on the surface (b).

III.3.5 – Behavior under vapor HF

As vapor HF etching constitutes the last operation, the behavior of the whole stack under this etchant must be investigated too, particularly concerning bonding oxide and interface. For this study, an exposition under vapor HF during 30min was performed on a quarter of sample just after direct bonding operation. Cross-sectional SEM observations were then performed (exposed in Figure III.3.30 and III.3.31). According to Figure III.3.30-c, bonding interface is affected and etched on almost 9µm. The distances etched after 30min of different materials present on the stack are depicted both on Figure III.3.31 and on Table III.9, which allows the determination of their etch-rate.

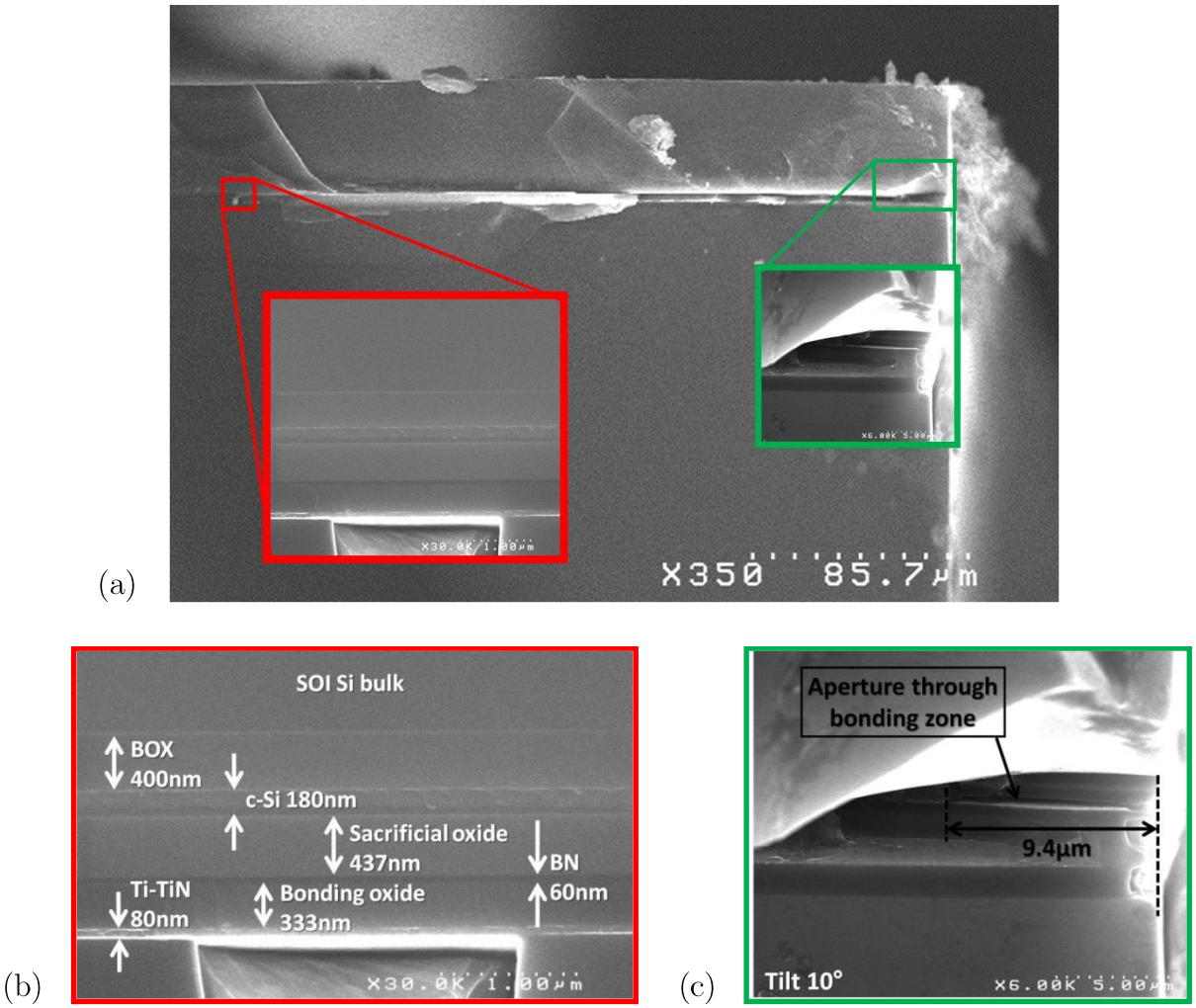


Figure III.3.30: Cross sectional SEM views of SOI-CMOS bonded wafers after a 30min exposition under vapor HF. General view (a) with focus on areas not affected (b) and affected (c) by HF agent.

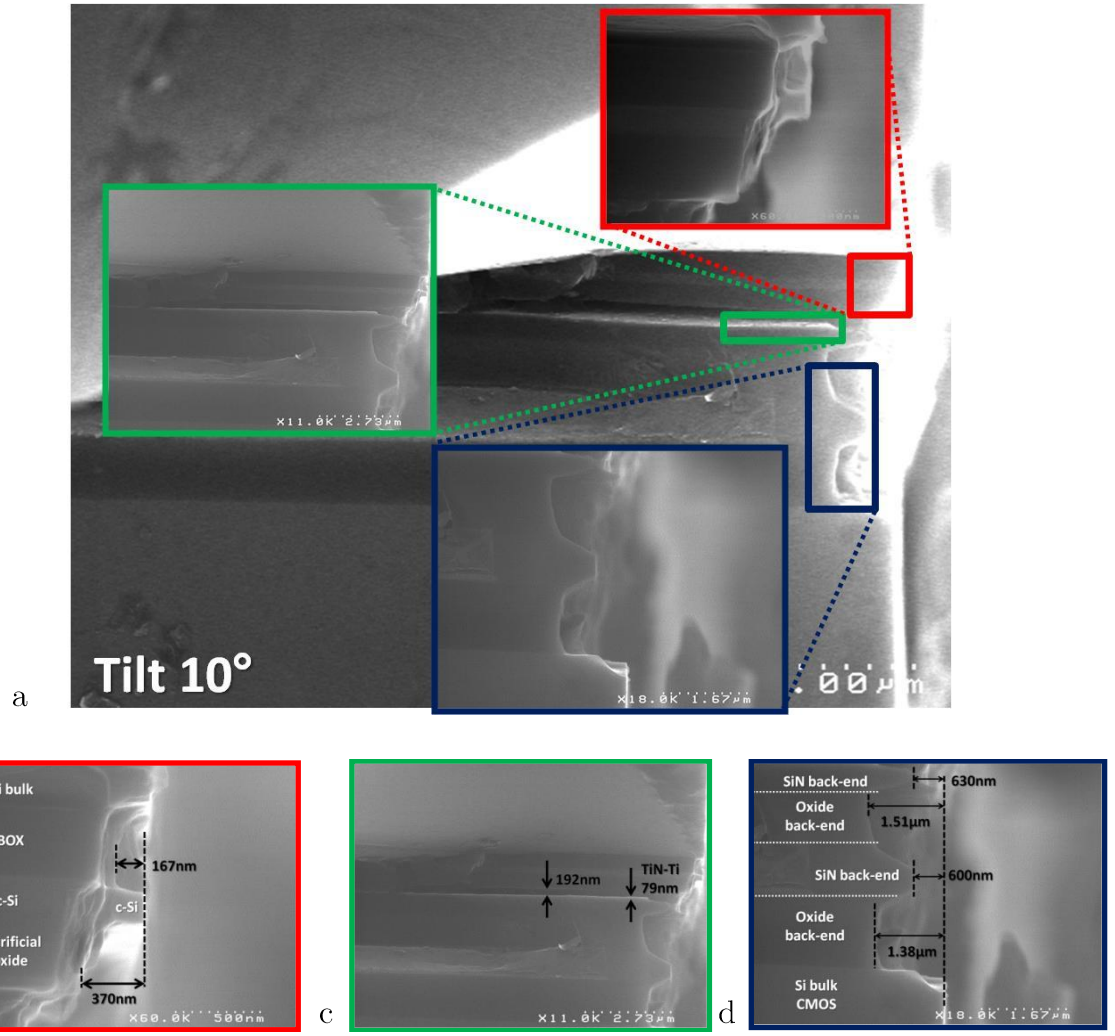


Figure III.3.31: Cross-sectional SEM views of zones affected by vapor HF etching. General view (a) with focus on SOI substrate (b), bonding oxide (c) and CMOS wafer (d).

Material	BOX	Sacrificial oxide	SiN back-end	Oxide back-end	TiN
Distance etched (nm)	167	370	600 – 630	1380 – 1510	0
Etch-rate (nm.min^{-1})	6	12	20 – 21	46 – 50	0

Table III.9: Etch-rate values for materials in CMOS-AMS stack under vapor HF for 30min.

The value obtained for the sacrificial layer (TEOS LR here) is consistent with the results obtained in section III.1. The different zones depicted in Figure III.3.31 show that TEOS-based oxide bonding is totally etched after 30min, which is expected according to the etch rates of Figure III.3.5.

IV. Discussion and conclusion

This chapter has dealt on the feasibility study of a 3D M/NEMS-CMOS system. The process flow analysis outlined and studied separately three major technological modules:

- The direct molecular bonding demonstrated the weakness point of the structure. The interface between the etch-stop and the bonding oxide layers appears to be fragile during the rough polishing and the vapor HF release. To avoid delamination, an improvement of this interface must be performed, for example by improving the cleanliness of the etch-stop layer surface after its deposition and its adherence with the bonding oxide layer;
- The NEMS resonator release study has shown that TEOS, TEOS LR and HDP SiH_4 constitute promising candidates for sacrificial layer, whereas BN and HfO_2 can be selected as etch-stop layer because of their outstanding resistance under vapor HF;
- WSi appears as a suitable material for the interconnection implementation between NEMS and CMOS since it does not react with vapor HF and since it can fill in high aspect ratio vias;

This approach is very interesting for monolithic NEMS-CMOS based sensors. Indeed, this oxide-oxide bonding only implies a few steps are necessary to build the entire stack, and low alignment requirements are necessary unlike direct metal-oxide bonding.

There is still much room for improvement. CMOS substrates with apertures in the back-end giving access to the last metal level were selected for the NEMS-CMOS interconnection development. Nevertheless, this choice leads to some planarization operations with a lot of constraints concerning the planarity for the molecular bonding. Furthermore, WSi constitutes a promising metal as it is deposited using CVD techniques and can fill in high aspect ratio vias. As a consequence, CMOS substrates without any apertures in the back-end would make easier the fabrication process since it would induce less problems of surface topography.

Technology	Monolithic integration			
	Below-IC	**In-IC**	**Above-IC (deposition approach)**	**Above-IC (direct molecular bonding approach)**
Advantages	- No encapsulation of the sensing part - Possible use of c-Si as structural material for MEMS - Low parasitic capacitances	- MEMS fabricated along the CMOS foundry process (in ME; BE configuration) - Interconnection material (good electrical conductor) - c-Si as structural material for MEMS (in FE configuration) - Low parasitic capacitances	- High flexibility with respect to the CMOS technology - Sensing part not encapsulated - Low area consumption - Low parasitic capacitances	- High flexibility with respect to the CMOS technology - Sensing part not encapsulated - c-Si as structural material for MEMS possible - No alignment requirement compared to direct metal-oxide bonding approach - Low parasitic capacitances
Drawbacks	- Interconnection compatible with FE (no use of Cu/Al) - Necessary modification of the CMOS process - Many fabrication steps	- Modification of CMOS process (in FE approach) - c-Si based MEMS not possible (in ME and BE approach) - No use of high temperature process - Encapsulation of the sensing part - Large area consumption - Necessary protection of the CMOS	- No use of high temperature process - c-Si based MEMS not possible - Necessary protection of the CMOS	- High planarity requirements - Necessary protection of the CMOS - Use of highly conformal, HF resistant metal for interconnection

Table III.10: Comparison between the different monolithic approaches.

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Chapter IV

Layout design considerations for monolithic NEMS-CMOS co-integration

Previous chapters demonstrated that monolithic co-integration between NEMS resonators and CMOS circuits constitute a promising solution to implement a high-performance mass sensor, in terms of fabrication process and electrical features. Layout considerations are a crucial point for the implementation of a sensor comprising a nano-resonators array and electronic circuits. This architecture must indeed maximize the sensor performance by increasing the capture cross-section and, at the same time, minimizes the area consumption which impacts on the detector fabrication cost. In this chapter the different dimensional constraints present for the sensor implementation are investigated. This investigation will allow to determine the size limit of a resonators array and to find possible solutions to improve its density.

I. Context

This layout design study will concern a certain kind of NEMS-CMOS devices with the following specificity:

- Nano-resonator are made up of c-Si;
- Structures used in this study are cross-beams, see section II.3 of chapter I;
- Electromechanical release is performed with vapor HF etching;
- Pads used for device characterization are not included here.

Three monolithic configurations fulfill these criteria: 2D NEMS-CMOS, 3D NEMS-CMOS with c-Si NEMS in ME, and 3D NEMS-CMOS above-IC. These integration schemes will be studied following a design consideration in subsequent sections, with an analysis of density-related constraints.

II. 2D NEMS-CMOS and 3D NEMS-CMOS with c-Si NEMS in ME

II.1 Introduction

As described in sections III.2.4.2 of chapter I and section I.2 of chapter III, both 2D and 3D NEMS-CMOS with c-Si NEMS in ME configurations (illustrated in Figures IV.2.1 and IV.2.2) show common features. Indeed, among all monolithic integration schemes, the interconnect length between NEMS and CMOS is the shortest one, since it may use only one metal layer to connect each other. Moreover an aperture through the back-end is necessary to have access to the electromechanical devices before the release step.

Six dimensions characterize the size of a NEMS array co-integrated with a CMOS circuit (see Figures IV.2.1 and IV.2.2):

- the distance between metal connections and NEMS resonator: $d_{metal\text{-}NEMS}$;
- the distance between two metal connections at the i^{th} level: $d_{metal\ i\ -metal\ i}$;
- the length and width occupied by a metal connection located at the i^{th} level: $L_{metal\ i}$ and $w_{metal\ i}$;
- the length and width occupied by back-end aperture down to the NEMS: L_{NEMS} and w_{NEMS}.

$d_{metal\ i\ -metal\ i}$ and $w_{metal\ i}$ have a minimum value which depends on the implemented CMOS technology. The other dimensions are free since NEMS pattern and release are performed out of the CMOS process. The minimum value of all these parameters depends on fabrication issues and electronic properties such as current leakage, parasitic cross-talk etc. The layout design of both sensing array and electronic circuit may be divided into two major parts: one concern constraints between electromechanical devices and metal connection and the other one concerns constraints between NEMS and CMOS circuit.

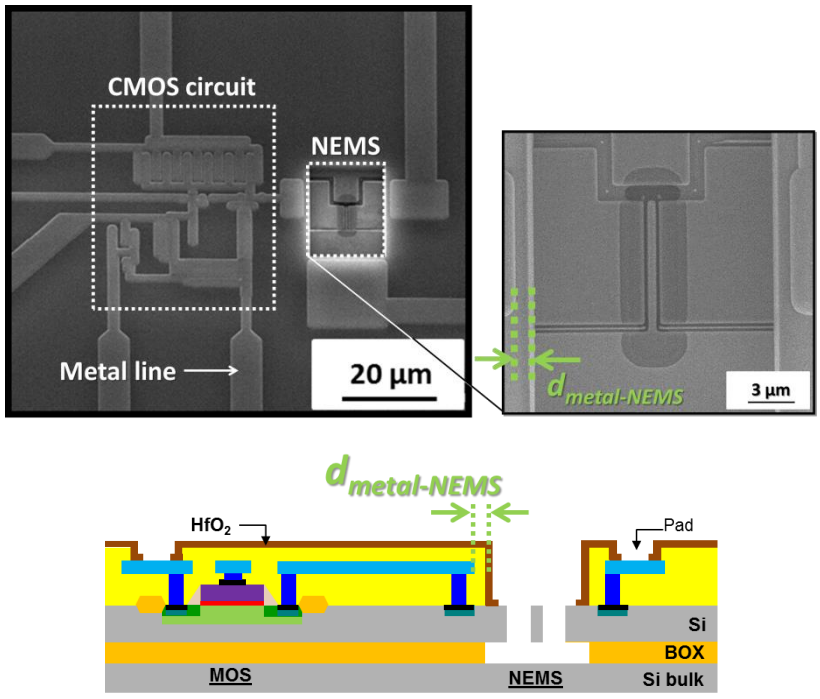
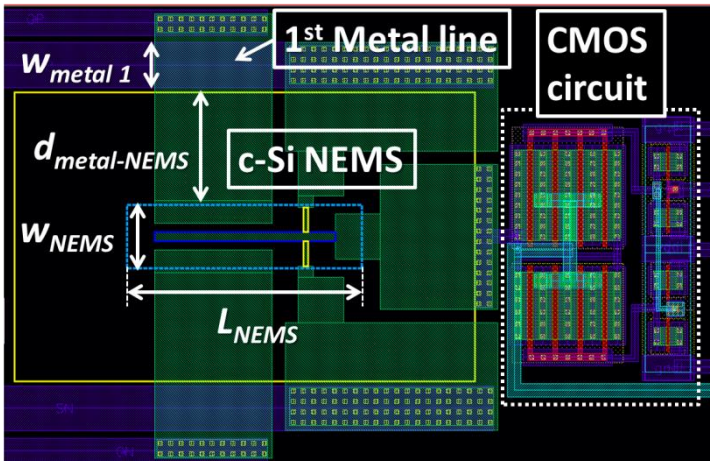


Figure IV.2.1: SEM micrograph top view (a) and cross-sectional schematic (b) of an example of a 2D monolithic NEMS-CMOS device [Arc12].

(a)



(b)

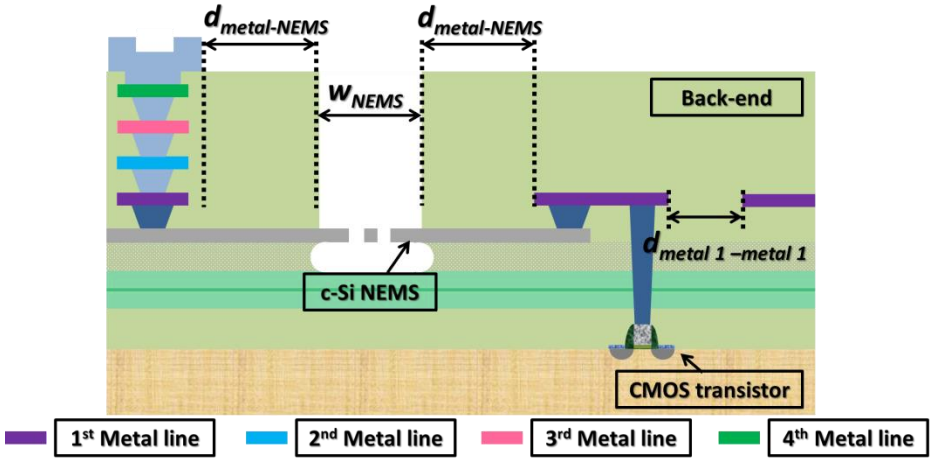


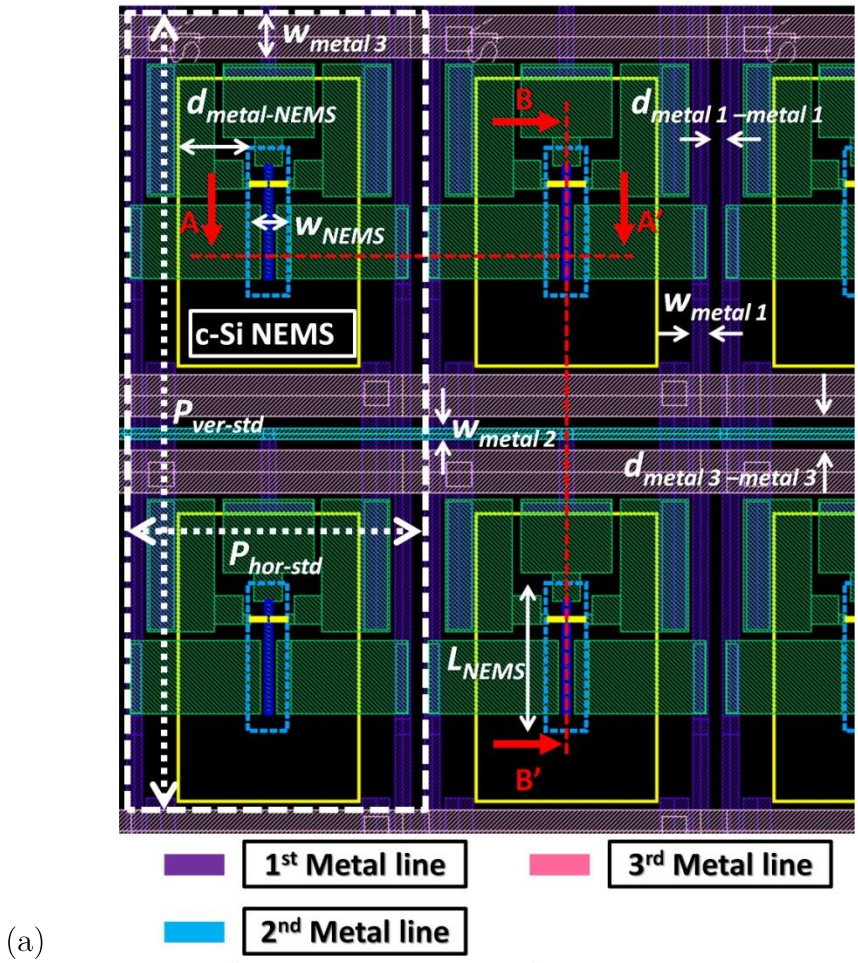
Figure IV.2.2: Layout top view (a) and cross-sectional schematic (b) of an example of a 3D monolithic NEMS-CMOS device with c-Si NEMS in ME.

II.2 NEMS and CMOS layout design consideration

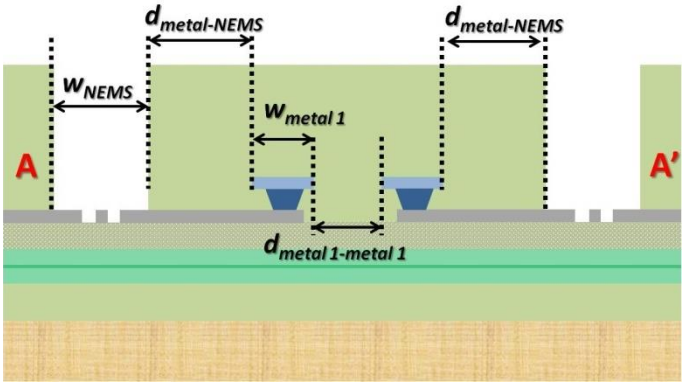
Metal interconnections likely impose the NEMS arrays density, *i.e.* the pitch $P_{NEMS\text{-}NEMS}$ between two different resonators. As observed in Figure IV.2.3, this pitch depends on several distances: $w_{metal\ i}$;$L_{metal\ i}$; $d_{metal\ i\ -metal\ i}$; w_{NEMS}; L_{NEMS} and $d_{metal\text{-}NEMS}$. This figure depicts a NEMS resonators array with four metal levels located above electromechanical devices. Dimensions ($L_{metal\ i}$ and $w_{metal\ i}$) of these metal layers are adequately selected to support the possible current density during sensor operation while respecting CMOS design rules, particularly for $d_{metal\ i\ -\ metal\ i}$ and $w_{metal\ i}$ dimensions.

2D and 3D NEMS-CMOS with c-Si NEMS in ME impose design rules concerning the apertures through the back-end, *i.e.* w_{NEMS} and L_{NEMS}. As vapor HF etching is performed during the release process, back-end metals must not be in contact to avoid any damage as described in section III.2 of chapter III. Furthermore, depositing and patterning an etch-stop layer for the interconnection protection are difficult since the four-metal levels imply back-end apertures etching with high aspect ratio, making difficult any lithography processes, more particularly the photoresist coating step. Therefore, solving this issue implies the respect of a safety distance $d_{metal\text{-}NEMS}$ between metal and apertures. All these dimensions (w_{NEMS}, L_{NEMS} and $d_{metal\text{-}NEMS}$) must be optimized to release all the mechanical structure without damaging the back-end. w_{NEMS} and L_{NEMS} typically correspond to resonator dimensions including mechanical beam and piezoresistive gauges. $d_{metal\text{-}NEMS}$ is determined according to the materials present in the back-end, their etch-rate under vapor HF and the necessary duration necessary to release the NEMS structures. As the back-end is processed under 450°C (see section III.2.1 of chapter I), the dielectric stack is very sensitive to vapor HF (see Table III.9 in section III.3.6 of chapter III), making $d_{metal\text{-}NEMS}$ very large and thereby increasing NEMS pitch. According to etch-rate data from section III.3.6 of chapter III, almost 30min of etching are necessary to remove the 400nm thick sacrificial oxide present below the c-Si layer. Supposing that back-end is made up of the same oxide, about 1.5µm would be laterally etched during the release process. Consequently, $d_{metal\text{-}NEMS}$ must be larger than this value in order not to damage interconnections.

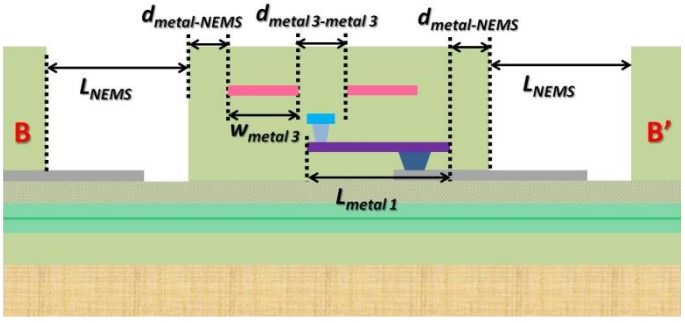
A possibility to build denser arrays would consist in sharing common electrodes and/or apertures of several NEMS devices as depicted in Figure IV.2.4. However, either for 2D and 3D ME NEMS-CMOS configurations, sensing part is fabricated alongside the electronic circuit, thus increasing the dimension of NEMS-CMOS cell.



(a)



(b)



(c)

Figure IV.2.3: Layout top view (a) and cross-sectional schematic (b-c) of an array of NEMS resonators before release.

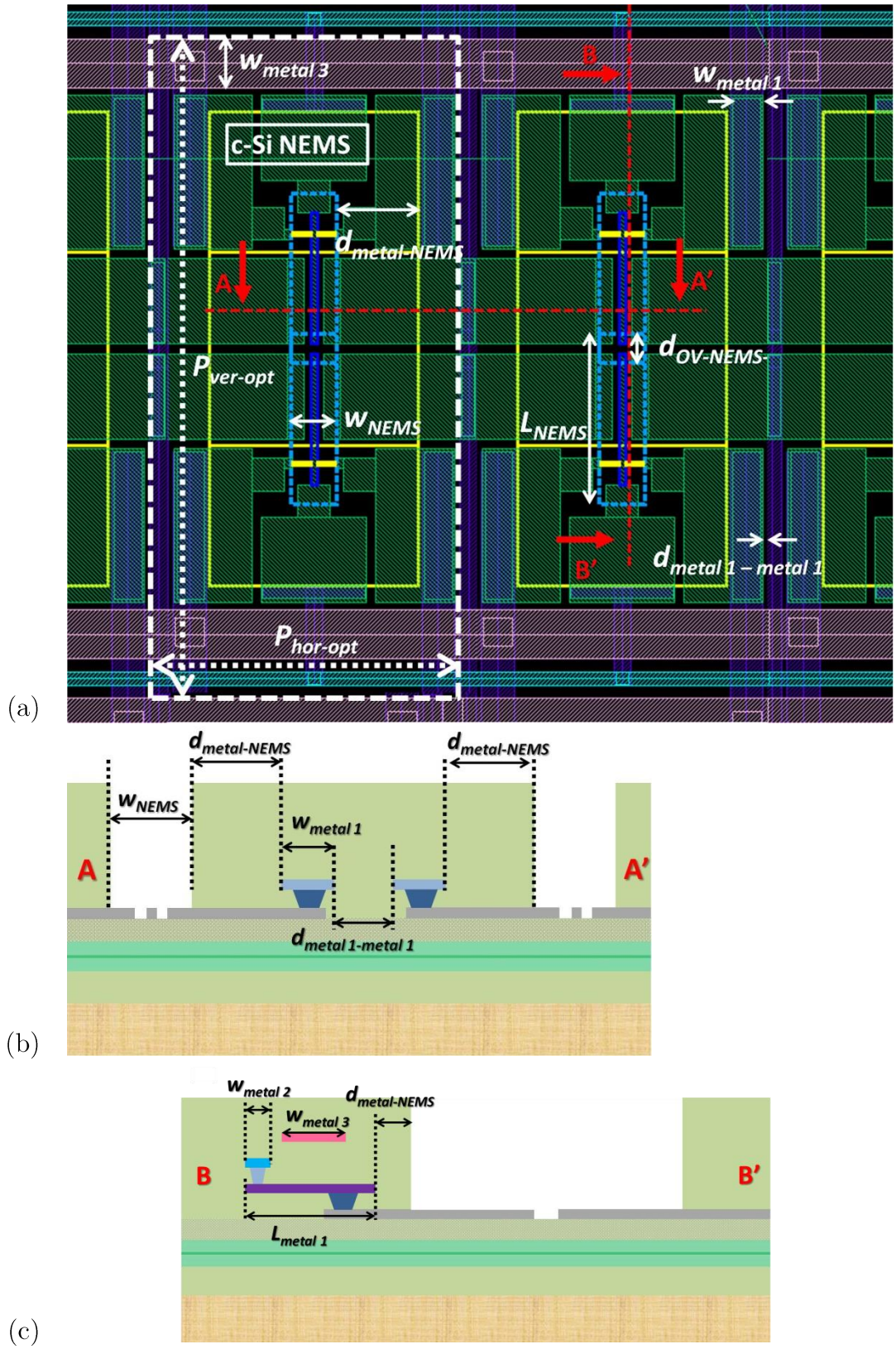


Figure IV.2.4: Layout top view (a) and cross-sectional schematic (b-c) of an array of NEMS resonators before release more densified by apertures and electrodes sharing.

II.3 Evaluation of the sensor compactness

This part focuses on the determination of the area occupied by the NEMS resonators. For this study, two 2-NEMS arrays designed following a standard and optimized layout respectively depicted in Figure IV.2.3 and Figure IV.2.4 are considered. The evaluation of the horizontal and vertical pitches (noted $P_{hor}$and P_{vert}) of these structures is first required. Their expressions are given below for standard (IV.1-2) and optimized (IV.3-4) architectures.

$$P_{hor-st} = 4w_{metal1} + 3d_{metal1-metal1} + 2d_{metal1-NEMS} + w_{NEMS} \ [\text{m}] \quad \text{(IV.1)}$$

$$P_{ver-st} = 3w_{metal3} + d_{metal3-metal3} + 4d_{metal3-NEMS} + 2L_{NEMS} \ [\text{m}] \quad \text{(IV.2)}$$

$$P_{hor-opt} = 3w_{metal1} + 2d_{metal1-metal1} + 2d_{metal-NEMS} + w_{NEMS} \ [\text{m}] \quad \text{(IV.3)}$$

$$P_{ver-opt} = 2w_{metal3} + d_{metal3-metal3} + 2d_{metal3-NEMS} + 2L_{NEMS} - d_{OV-NEMS-NEMS} \ [\text{m}] \quad \text{(IV.4)}$$

The different values for each dimension are described in Table IV.1. They take into account the NEMS resonator dimension described in Table III.2. The pitches evaluation allows the determination of the 2-NEMS array area and number with the number of NEMS resonators present on a die with a size of 1mm² thanks to expressions (IV.5), (IV.6) and (IV.7).

$$A_{2-NEMS-array} = P_{hor} \cdot P_{ver} \ [\text{m}^2] \quad \text{(IV.5)}$$

$$N_{2-NEMS-array} = \frac{A_{die}}{A_{2-NEMS-array}} \quad \text{(IV.6)}$$

$$N_{NEMS} = 2 \cdot N_{2-NEMS-array} \quad \text{(IV.7)}$$

Name	L_{NEMS}	w_{NEMS}	$d_{metal\ i\ -\ metal\ i}$	$w_{metal\ i}$	$d_{metal\ i\ -\ NEMS}$	$d_{OV\text{-}NEMS\text{-}NEMS}$
Value [µm]	15	1	0.5	0.5	1.5	1

Table IV.1: Values of dimensions taken for the pitch analysis.

All these values are summarized in Table IV.2. By sharing common electrodes and back-end apertures, a 24% decrease of the area occupied can be achieved.

Integration		**2D NEMS-CMOS and ME 3D NEMS-CMOS**
Standard layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}st}$ = 7.5µm $P_{vert\text{-}st}$ = 38µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	285µm² / 3508
	Maximum number of NEMS resonators on a 1mm² size die	7016
Optimized layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}opt}$= 6.5µm $P_{vert\text{-}opt}$= 33.5µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	217.75µm² / 4592
	Maximum number of NEMS resonators on a 1mm² size die	9184

Table IV.2: Area characteristics of NEMS arrays in 2D and ME 3D NEMS-CMOS devices.

II.4 Conclusion

The design of 2D or ME 3D NEMS-CMOS arrays faces two major issues. First, this method is expensive, since area is lost due to the safety distance $L_{metal\text{-}NEMS}$ for back-end protection from NEMS release, consequently decreasing the sensor compactness. Second, as both parts are located side by side, NEMS array is affected by a reduction of capture cross-section for molecules detection, thereby decreasing the sensor performance. Even if electrical interconnects between NEMS and CMOS are short, another integration scheme must be investigated in order to overcome these issues.

III. 3D NEMS-CMOS above-IC using direct oxide-oxide bonding

III.1 Introduction

As detailed in section II.2.2 of chapter III, 3D above-IC integration requires an SOI wafer and a full CMOS substrate. After the molecular bonding, NEMS resonators are patterned on top c-Si layer of the SOI wafer, then interconnected to the last back-end metal layer, as described in section II.2.3 of chapter III.

The sensing part being implemented above the electronics, a high density of NEMS is consequently expected. This section provides some guidelines to maximize this density, *i.e.* to get a higher capture cross-section. Figure IV.3.1 depicts a cross-sectional view of the final stack.

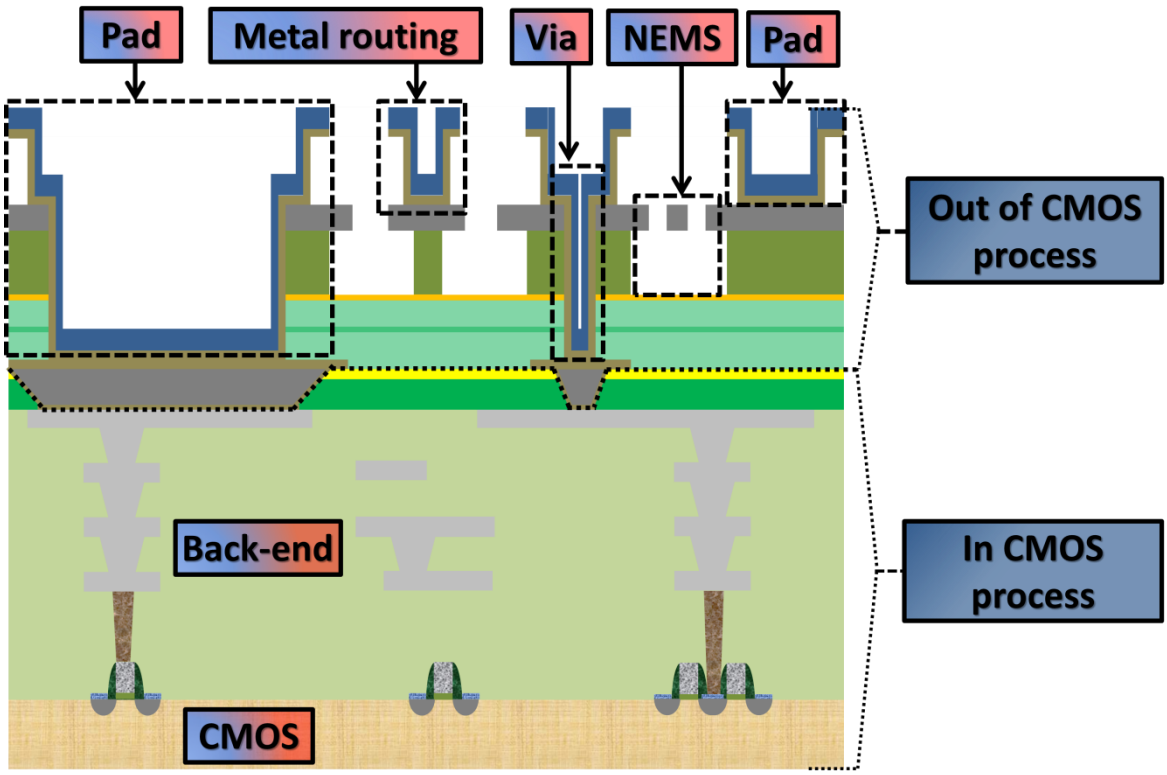


Figure IV.3.1: Cross-sectional schematic of a 3D NEMS-CMOS above-IC co-integration. Indications on the right show if fabrication occurs during or out the CMOS process, leading to different design rules for each layer.

III.2 CMOS Back-end

Figure IV.3.2 shows that two dimensions may have an impact on NEMS array density: width of metal line $w_{metal\ 4}$ and separation between two different routing $d_{metal4\ -\ metal\ 4}$. As explained in section I.1, these dimensions have a minimum value imposed by the foundry corresponding to either fabrication constraints or electrical properties issues.

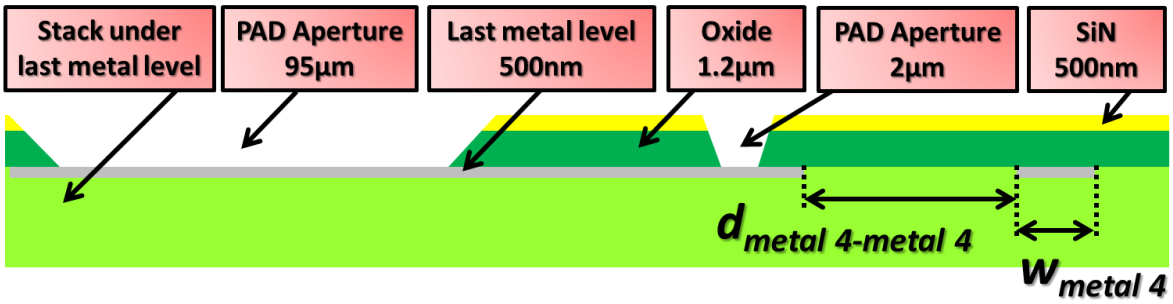


Figure IV.3.2: Cross-sectional schematic of a CMOS substrate before assembly.

III.3 Alignment between NEMS and CMOS substrates

In chapter II was explained that molecular bonding constitutes a promising approach since it does not imply any critical alignment requirements of substrates. Only primary marks are necessary for this purpose, allowing the fabrication of electromechanical devices and their interconnections with CMOS back-end. These marks have a typical size close to 100µm. Because of its large dimensions, the removal of c-Si in these zones is not critical from a dimensional point of view and does not affect sensor compactness on a die.

III.4 NEMS fabrication

Unlike other approaches studied in previous sections, apertures are not necessary for the release process. Indeed, the whole passivation oxide layer deposited after NEMS patterning is removed, and the metal used for interconnecting NEMS and CMOS does not react with vapor HF. Consequently, the safety distance is useless in this case, and the pitch between two NEMS resonators is reduced. However, fabrication of this interconnection becomes the most crucial step.

Three main parameters have to be investigated:

- Alignment with back-end apertures
- Contact area with c-Si layer
- Type of interconnect material

III.4.1 – Alignment with back-end apertures

The process flow presented in section III.2.3 of chapter III shows that vias etching and filling are necessary for interconnecting both NEMS and CMOS. These vias must be aligned with respect to the back-end. As depicted on Figure III.1.1 in chapter III, the alignment depends on interconnection dimensions: the narrower this via is, the better the alignment accuracy is. It is therefore recommended to work with vias as small as possible (characterized by their width w_{via}). Furthermore, an enclosure $d_{bar\text{-}via}$ of TiN barrier area with respect to vias can be performed in order to solve any misalignment problem. This enclosure is however limited by the minimum possible distance $d_{bar\text{-}bar}$ between two TiN barriers. All these dimensions will impose the minimum pitch $P_{via\text{-}via}$ between two different vias, as illustrated on Figure IV.3.3.

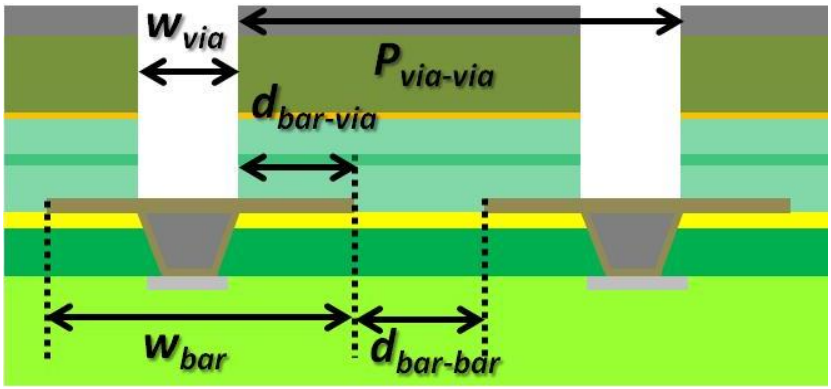


Figure IV.3.3: Cross-sectional representation of the different important dimensions for via design.

III.4.2 – Contact area with c-Si layer

Another important parameter is the contact area between metal and c-Si layer before via etching, particularly for piezo-resistive detection whereby contact resistance R_c are if primary concern. R_c is defined as:

$$R_c = \frac{\rho_c}{S_c - S_v} \ [\Omega] \tag{IV.8}$$

whereρ_c is the contact resistivity between metal and silicon (in $\Omega.m^2$) and $S_c$and S_v respectively correspond to the area of opened silicon area and via (in m^2). This contact resistance has to be as small as possible to avoid signal attenuation and Johnson noise. According to (IV.8), the contact resistance can be reduced by selecting suitable metallurgy with a low contact resistivity contact with silicon and/or by increasing the contact area. Nevertheless, the latter is confronted to the minimum achievable space (noted $d_{met\text{-}met}$ on Figure IV.3.4) between two metal interconnects (so-called metal pads in Figure IV.3.4). This parameter may differ according to the metal thickness t_{met} (see next section).

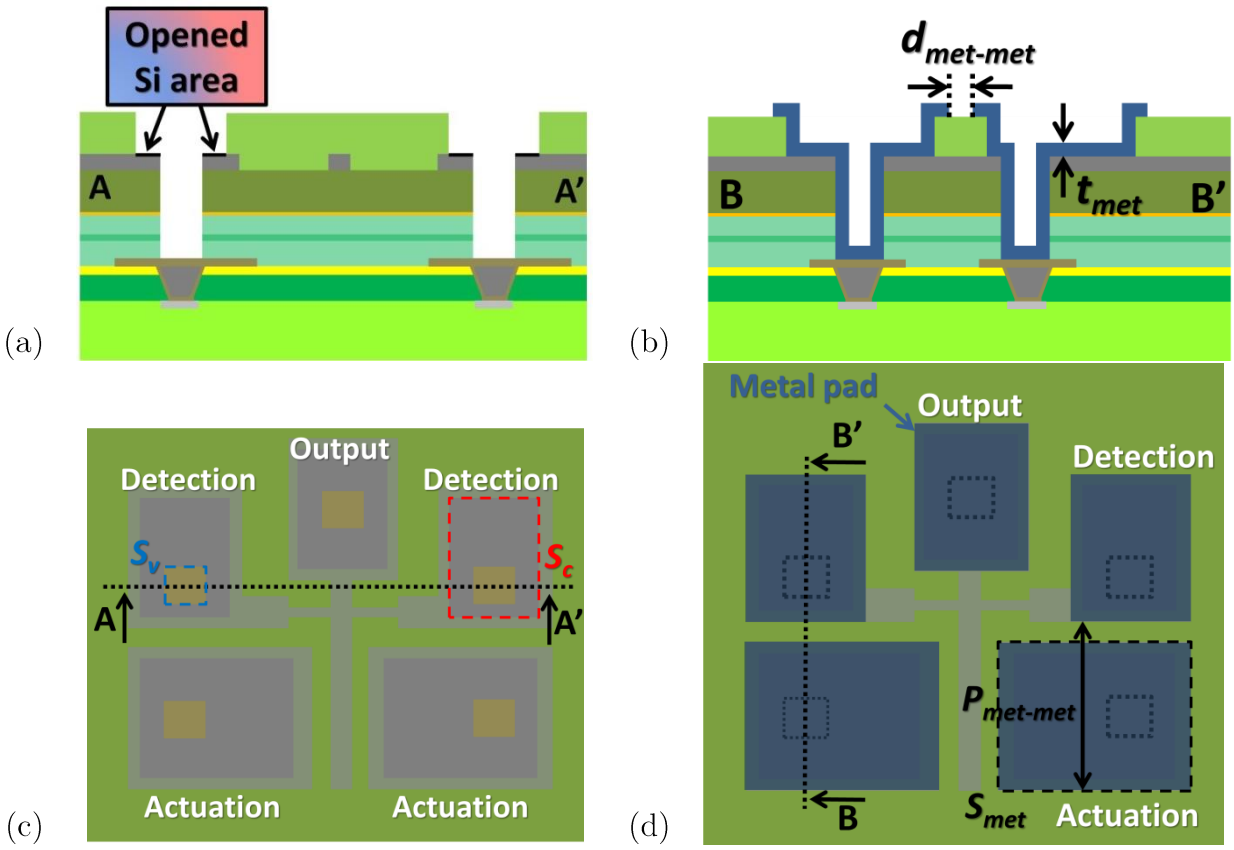


Figure IV.3.4: Cross-sectional (a-b) and top views (c-d) of NEMS devices array before (a-c) and after (b-d) metal deposition and patterning.

III.4.3 – Metal as interconnect

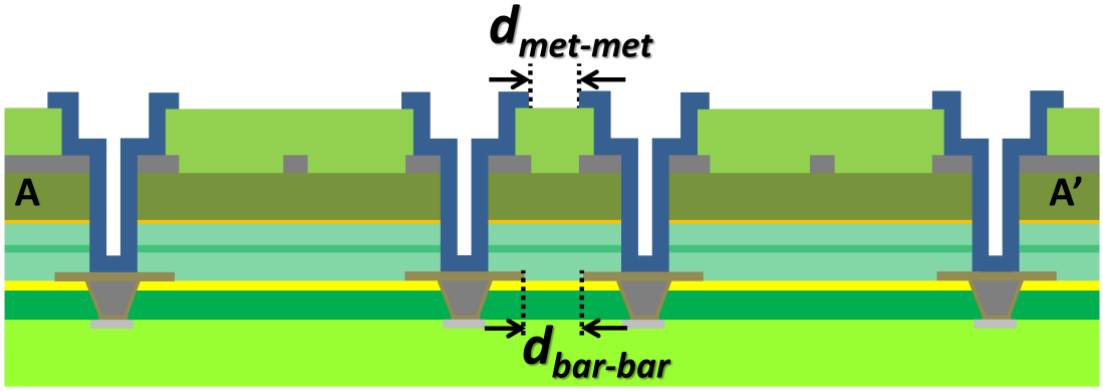
The metal thickness t_{met} constitutes a major parameter for NEMS density. This thickness may vary according to the deposition technique. As described in section III.2.2 of chapter III, a thick deposition of AlSi (more than 3µm) by PVD is necessary for contacting c-Si and Cu through vias with an aspect ratio smaller than one. Better results are obtained with WSi deposited by CVD which is conformal and requires some hundreds of nanometers to ensure electrical contact. After deposition, this metal is patterned. During this operation, photoresist is deposited at a similar thickness to protect some areas from etching. This thickness affects both resolution and minimum space between metal layers [Mad02]. Consequently, the thinner the metal deposition is, the thinner the photoresist is, the shorter $d_{met\text{-}met}$ is, and the better the density is.

Moreover, the previous section has shown that contact resistance is inversely proportional to $S_c - S_v$. To keep the same R_c,a reduction of via size allows a reduction of contact size too, leading therefore to a reduction of metal area S_{met} and a reduction of pad pitch $P_{met\text{-}met}$ (see Figure IV.3.4). This analysis confirms the convenience of CVD metals as interconnect.

III.5 NEMS array design optimization

All the main design constraints have been investigated for NEMS fabrication. Without taking into account back-end restrictions, two dimensions have to be taken particularly into account for nano-resonators array design: minimum pitches of TiN barrier (noted $d_{bar\text{-}bar}$) and interconnect metal (noted $d_{met\text{-}met}$). These dimensions both affect the device size itself (device and pads) and the array one. Figure IV.3.5 illustrates a typical NEMS resonators array. All elements of nano-resonators (*i.e.* actuation, detection and output) are interconnected with CMOS back-end through vias. Like in the first part of this chapter, it is possible to increase the array density by sharing common pads of devices, as illustrated in Figure IV.3.6 where actuation electrodes and two nanowire gauges of the resonators are connected with back-end through common vias.

(a)



(b)

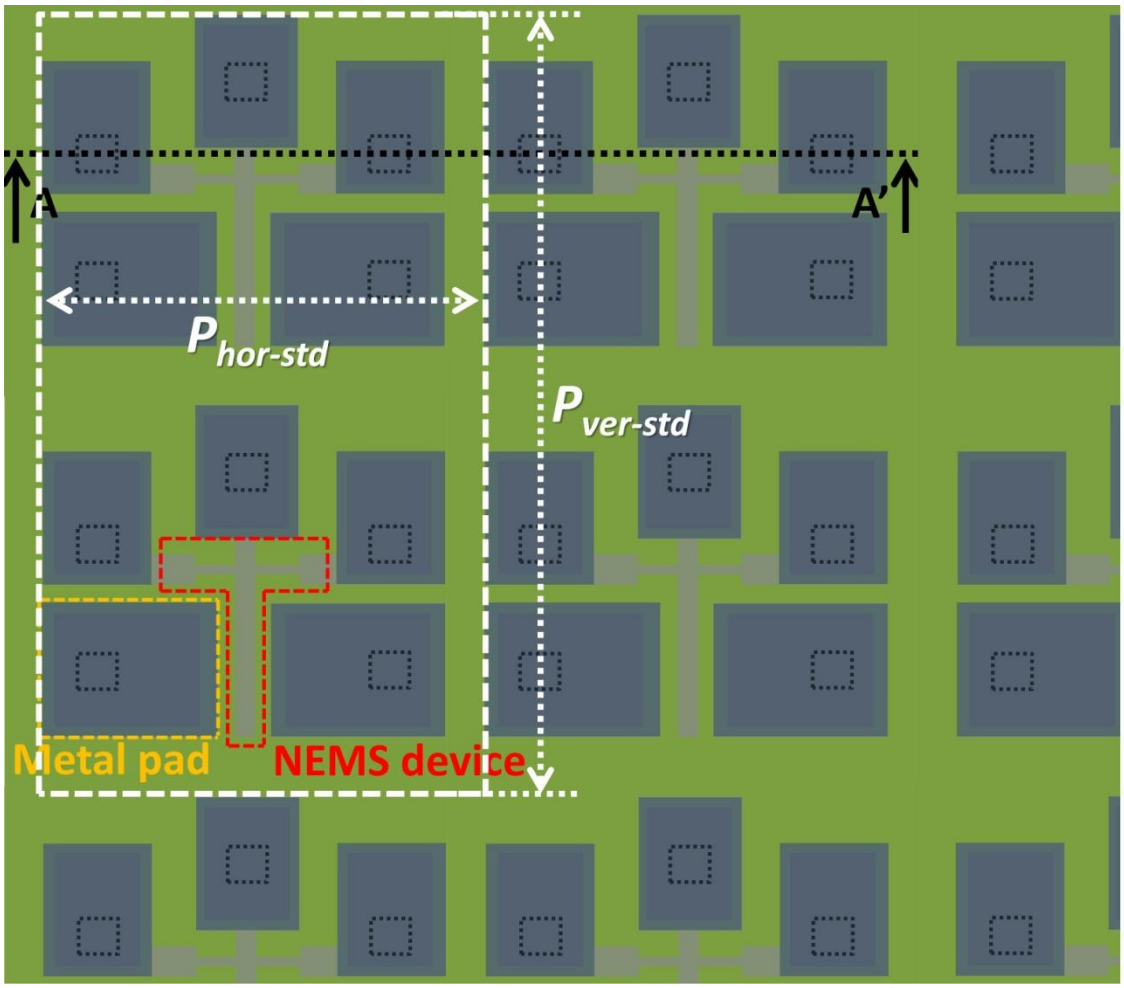
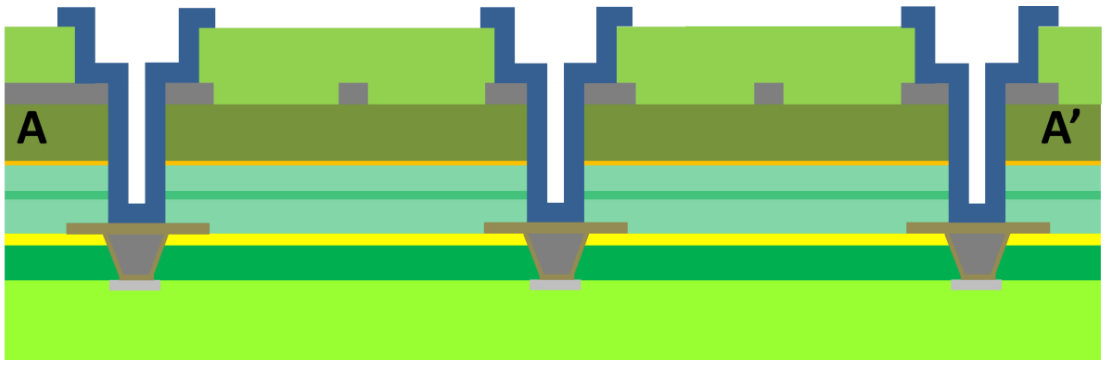


Figure IV.3.5: Cross-sectional (a) and top view (b) of a standard NEMS array.

(a)



(b)

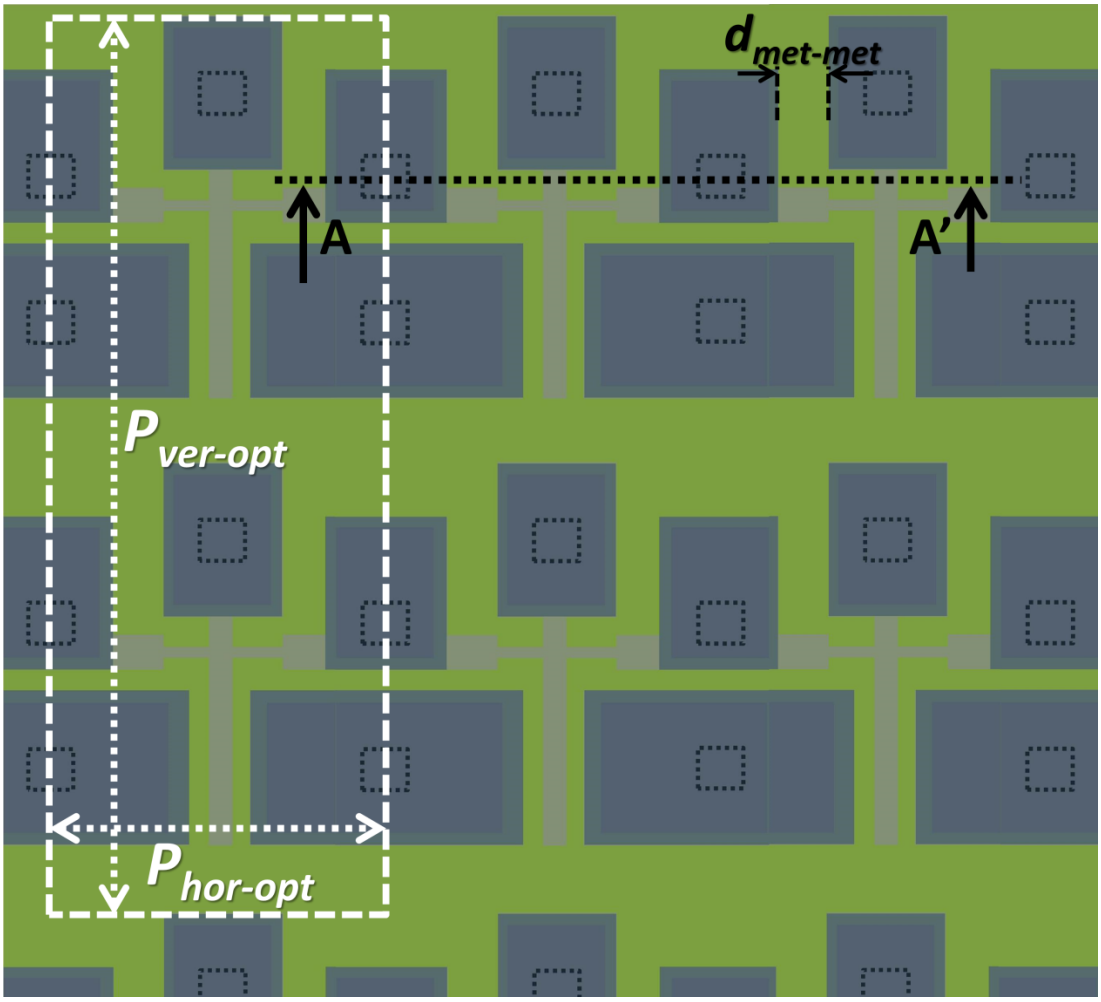


Figure IV.3.6: Cross-sectional (a) and top view (b) of a NEMS array with common contact (here actuation electrodes and two nanowire gauges are shared by two different devices).

III.6 Evaluation of the sensor compactness

The analysis presented in II.3 is conducted for 3D NEMS above-IC with a standard and an optimized architecture respectively illustrated in Figure IV.3.5 and IV.3.6. The expressions of the different horizontal and vertical pitches are given below. The metal pads for the detection, actuation and output parts are considered as squares with an area S_c.

$$P_{hor-st} = 2\sqrt{S_{met}} + d_{metal-metal} + w_{NEMS} \quad \text{(IV.9)}$$

$$P_{ver-st} = 2\sqrt{S_{met}} + 2L_{beam} + 2d_{metal-metal} \quad \text{(IV.10)}$$

$$P_{hor-opt} = \sqrt{S_{met}} + w_{NEMS} \quad \text{(IV.11)}$$

$$P_{ver-opt} = 2\sqrt{S_{met}} + 2L_{beam} + 2d_{metal-metal} \quad \text{(IV.12)}$$

The different values for each dimension are described in Table IV.3. As investigated in II.3, the 2-NEMS array area and the number of NEMS resonators present on a die with a size of 1mm^2 are determined using expressions (IV.5); (IV.6) and (IV.7).

Name	L_{beam}	w_{NEMS}	$d_{metal-metal}$	$\sqrt{S_{met}}$
Value [µm]	10	1	0.5	2

Table IV.3: Values of dimensions taken for the pitch analysis.

All these values are summarized in Table IV.4. By sharing common actuation and detection electrodes, a 45% decrease of the area occupied can be achieved.

Integration		3D NEMS above-IC
Standard layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}st}$ = 5.5µm $P_{vert\text{-}st}$ = 25µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	137.5µm² / 7272
	Maximum number of NEMS resonators on a 1mm² size die	14544
Optimized layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}opt}$= 3µm $P_{vert\text{-}opt}$= 25µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	75µm² / 13333
	Maximum number of NEMS resonators on a 1mm² size die	26666

Table IV.4: Area characteristics of NEMS arrays in 3D above-IC configuration.

IV. Discussion and conclusion

This chapter proposes a brief analysis on the layout design of a NEMS array co-integrated with CMOS circuit. The driving parameters of NEMS array density were identified for each kind of monolithic integration schemes. The monolithic 3D above-IC approach appears to constitute the most optimal option for the creation of dense arrays of resonators since CMOS back-end is located below the NEMS devices and is protected by an etch-stop layer. This is demonstrated by the maximum possible number of NEMS resonators on a 1mm² size die. The values depicted in Table IV.5 shows that 3D above-IC approach allow the fabrication of an array more than twice dense as the ME 3D NEMS-CMOS one. Moreover, as the CMOS circuit is placed below the NEMS array, the area occupied by the whole sensor can be considerably smaller than in a 2D or a ME 3D NEMS-CMOS integration.

Integration		2D NEMS-CMOS and ME 3D NEMS-CMOS	3D NEMS above-IC
Standard layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}st}$ = 7.5µm $P_{vert\text{-}st}$ = 38µm	$P_{hor\text{-}st}$ = 5.5µm $P_{vert\text{-}st}$ = 25µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	285µm² / 3508	137.5µm² / 7272
	Maximum number of NEMS resonators on a 1mm² size die	7016	14544
Optimized layout	Pitch between two 2-NEMS arrays	$P_{hor\text{-}opt}$= 6.5µm $P_{vert\text{-}opt}$= 33.5µm	$P_{hor\text{-}opt}$= 3µm $P_{vert\text{-}opt}$= 25µm
	Area and maximum number of 2-NEMS array on a 1mm² size die	217.75µm² / 4592	75µm² / 13333
	Maximum number of NEMS resonators on a 1mm² size die	9184	26666
Area of NEMS-CMOS device		$A_{NEMS\text{-}array} + A_{CMOS}$	$A_{NEMS\text{-}array}$ or A_{CMOS}

Table IV.5: Summary of area characteristics for different integration scheme and different kind of layout. $A_{NEMS\text{-}array}$ and A_{CMOS} respectively corresponds to the area occupied by the NEMS array and the CMOS circuit.

Bibliography of chapter IV

[Arc12] J. Arcamone, M. Savoye, G. Arndt, J. Philippe, C. Marcoux, E. Colinet, L. Duraffourg, T. Magis, M. Laurens, A. Monroy-Aguirre, P. Mazoyer, P. Ancey, P. Robert and E.Ollier, *VLSI platform for the monolithic integration of single-crystal Si NEMS capacitive resonatos with low-cost CMOS*, IEDM 2012.

[Mad02] M. J. Madou , *Fundamentals of microfabrication: the science of miniaturization*, 2nd ed., CRC Press, New York, NY.

Conclusions and perspectives

Transitioning from a theoretical concept to concrete and real devices, MEMS have become very promising objects during the last 50 years. After many technological improvements including the development of processes compatible with CMOS technology, MEMS are now present in numerous applications in our daily life. Pioneered since a decade, the sub-µm downscaling of micrometric size objects has allowed the emergence of NEMS. Their nanometer size makes possible the use of electromechanical systems for specific applications requiring a high level of sensitivity and resolution generally, such as gas sensing and mass detection. NEMS resonator structures constitute suitable devices for such applications. By tracking the resonance frequency evolution of the movable cantilever over time, the determination of the mass deposited on the beam can be determined with an outstanding resolution. However, a CMOS electronic circuit is necessary to constitute a real-time sensor. This circuit is used both as the readout part at the output of the NEMS, and as a sustaining feedback amplifier for the oscillating-loop implementation with the nano-resonators.

In chapter I, diverse techniques were described for the integration of NEMS devices with CMOS circuit. All of them can be classified into two main groups: the hybrid (or stand alone) and the monolithic integration (so-called co-integration) which respectively consists in processing NEMS and CMOS on separate and same die. The hybrid techniques greatly simplify sensor fabrication since every element can be manufactured without impacting on the implementation of the other one. Nevertheless, the monolithic strategy appears as the best option in terms of electrical performance. Additionally, only a few more fabrication steps are required compared to hybrid integration. Many possibilities exist in the co-integration strategy according to the position occupied by the nano-resonators in the CMOS stack, which imposes the maximal achievable temperature for the NEMS process.

The signal transmission properties of different integration approaches investigated in the first part of the chapter II showed that the 3D interconnects, the direct metal-oxide bonding approach and the monolithic integration almost do not degrade the electrical signal between NEMS and CMOS, unlike TSVs and wire-bonding techniques. Chapter II also presented the modeling and the experimental characterization of a 2D NEMS capacitive resonator co-integrated with a compact and low-cost CMOS circuit. These two elements are both processed on the top c-Si layer of an SOI substrate. The open-loop characterization of the CMOS circuit and the NEMS-CMOS system allowed the extraction of some characteristic parameters of the resonator (e.g. the quality factor and the resonance frequency), the circuit (gain in

function of the supply voltage) and the parasitic elements (feedthrough signal and parasitic interconnection capacitance). All these results made possible the implementation of a very compact (maybe the most compact one) NEMS-CMOS self-oscillating loop. By fabricating a large array of such a structure, this architecture could constitute a promising device for mass sensing application. It is however possible to decrease the area consumed by switching from a 2D to a 3D NEMS-CMOS structures. This particular strategy was studied in the third chapter.

To implement NEMS resonators using electrostatic actuation and piezoresistive detection (so-called cross-beams), the best material is c-Si since it provides an outstanding piezoresistive gauge factor compared to other materials (metals for example). For the fabrication of mass sensors based on c-Si nano-resonators, a process flow was developed and studied following a 3D above-IC approach where the NEMS part is processed above both the CMOS circuit and the back-end interconnections. A direct oxide-oxide bonding between an SOI wafer and a CMOS substrate with the use of c-Si top layer from the SOI one as structural layer for NEMS devices make possible such integration. All the high temperature processes required for NEMS fabrication (i.e. thermal annealing after doping step) are managed before the assembly. Three main technological modules were indentified and carefully investigated.

- The final release of the mechanical structure with vapor HF requires the use of two different layers: a sacrificial layer which surrounds the resonator, and an etch-stop layer to protect the back-end during the operation. TEOS, TEOS LR and HDP SiH_4 appear to be excellent candidates as sacrificial material whereas BN and HfO_2 are promising etch-stop layers;
- Another critical module concerns the electrical connection between the c-Si NEMS and the back-end interconnections. Among several possibilities, WSi constitutes an outstanding solution since it is not affected by vapor HF and since it fills in vias even with strong aspect ratio.
- The last and the most critical step concerns the molecular bonding between the SOI and the CMOS substrates. The results obtained after the polishing step of the SOI substrate showed some delamination which might come from the interface between the etch-stop layer and the bonding oxide. This could be due to either a low interface energy, or the presence of particles, or the planarity affecting the bonding oxide topography. Some works are necessary to improve this interface.

It is however possible to optimize this integration. The outstanding conformal properties of WSi make possible the use of non-opened CMOS wafers, reducing thereby the number of steps and simplifying the planarization process before the molecular bonding. Another perspective would be the use of material deposition steps without any SOI substrates and without any expensive bonding process to implement the stack. This strategy imposes a maximal temperature below 450°C for the nano-resonators fabrication limiting consequently the temperature of the material deposition and the thermal annealing. Nevertheless, both the thermal activation and diffusion of the dopants could be performed through laser annealing without impacting the back-end stack.

In order to increase the capture area to collect the largest number of molecules and thereby to improve the precision of the NEMS-based sensor, the fabrication of a large array of nano-resonators appears as an optimal solution. Consequently, the design of such an array constitutes a crucial part in order to achieve a compact detector. The analysis performed in the chapter IV showed that 3D above-IC allows the integration of a larger number of nano-resonators than 2D or 3D ME NEMS-CMOS schemes. Moreover, it is possible to further increase the NEMS density by sharing common actuation and detection electrodes. It is necessary to verify the functionality of such strategy. Indeed, the damaging of one resonator could deeply affect the performance of the entire array, possibly making this disposition less effective than the standard one without any electrodes sharing. A further analysis of the trade-off between efficiency and density of this array is thereby required.

In this thesis, several aspects of the co-integration between NEMS and CMOS were investigated, particularly the technological assembly, the electronic architecture and the design strategy. The analysis of the fabrication process of 3D above-IC monolithic integration, the layout design study of a dense NEMS array and the experimental demonstration of a compact NEMS-CMOS self-oscillator pave the way for promising high-performance mass sensors based on NEMS devices.

Introduction Générale

Ces dernières décennies ont vu l'émergence des microsystèmes électromécaniques (MEMS) grâce notamment aux techniques de fabrication employées dans l'élaboration des transistors. L'utilisation de différentes propriétés physiques (électroniques, mécaniques, optiques par exemple) a permis la construction d'un large panel de capteurs et d'actionneurs miniaturisés rendant ces systèmes électromécaniques omniprésents dans notre vie quotidienne, par exemple dans nos voitures (airbags, capteurs de pression) ou dans nos smartphones (microphones, accéléromètres). Dans les années 2000, la miniaturisation submicronique des MEMS a conduit à l'émergence d'un nouveau type de dispositifs : les NEMS (Nano Systèmes Electro Mécaniques). Bien que ces dispositifs de taille nanométrique ne prétendent pas aux mêmes applications que les systèmes de dimension micrométrique, leurs excellentes propriétés rendent possible l'utilisation de ces systèmes électromécaniques dans des applications spécifiques nécessitant un haut niveau de sensibilité et de résolution, comme la détection de gaz, la spectrométrie de masse et la reconnaissance des molécules, faisant traditionnellement appel à des machines volumineuses. Pour ce type d'application, un circuit électronique de type CMOS est nécessaire à l'élaboration d'un capteur en temps réel, et ce pour deux raisons principales:

- ❖ Améliorer la lecture du signal en sortie de NEMS sans dégradation du signal;

- ❖ Réaliser une boule fermée (comme une boucle à verrouillage de phase ou une boucle auto-oscillante) permettant la mesure de masse en temps réel.

L'intégration du circuit électronique avec les NEMS constitue un point critique pour la fabrication de capteurs compacts et de haute performance.

Le travail présenté dans ce manuscrit a été réalisé dans le cadre d'un projet ERC (European Research Council) appelé DELPHINS (Design and ELaboration of multi-Physics Integrated NanoSystems). L'objectif principal vise au développement d'un design et d'une technologie de fabrication d'une plate-forme générique sur puce constituée de capteurs multi gaz pour les applications d'analyses embarqués, capteurs basés sur des réseaux de résonateurs NEMS en tant que dispositifs de détection. Cette thèse présente une mise en œuvre technologique originale pour atteindre ce but.

Le premier chapitre de ce manuscrit présente le contexte général des dispositifs M/NEMS, suivi d'un aperçu des solutions existantes pour l'application de détection de masse. Le principe de fonctionnement d'un résonateur NEMS pour la détection de

masse sera également décrit. Dans une dernière partie, les différentes méthodes permettant d'intégrer les NEMS avec les circuits CMOS seront présentées.

Dans le chapitre II, les principaux résultats de caractérisations électriques d'un dispositif à base de résonateur NEMS co-intégré CMOS seront présentés. Une modélisation de ce système est également proposée et est utilisée pour extraire les paramètres et les performances du résonateur. A partir de ce modèle et des résultats électriques, une démonstration expérimentale d'une boucle d'auto-oscillante est présentée.

Le troisième chapitre proposera une nouvelle méthode pour la fabrication d'un détecteur de masse en utilisant une co-intégration 3D dans laquelle les résonateurs de type NEMS sont fabriqués de façon monolithique au-dessus du circuit CMOS et des interconnexions (intégration dite « above-IC ». Le processus de fabrication et les principales briques technologiques seront expliqués.

Avant la conclusion, le chapitre IV fournira brièvement quelques lignes directrices pour optimiser la mise en place d'un grand réseau de résonateurs NEMS co-intégrés CMOS.

Chapitre I

Micro et Nano Systèmes Electro Mécaniques
Dispositifs prometteurs pour la fabrication de capteurs performants

Les micro et nano systèmes électromécaniques (ou M/NEMS) correspondent à des objets de taille micro et nanométrique utilisant de multiples propriétés physiques de la matière, telles que électroniques, mécaniques, thermiques, optiques, magnétiques etc. Le matériau principalement utilisé pour la fabrication de ces M/NEMS est le silicium pour son très faible coût d'exploitation (élément très abondant sur Terre) ainsi que pour ses propriétés électroniques et mécaniques remarquables. En outre, les procédés de traitement du silicium pour la fabrication des systèmes électromécaniques sont les mêmes que ceux utilisés en microélectronique pour l'élaboration des transistors CMOS (Complementary Metal Oxide Semiconductor). Par conséquent, les structures électromécaniques constituent des objets très attractifs en raison de leur potentiel d'intégration à très grande échelle et leur compatibilité avec la technologie CMOS.

I. Introduction

I.1 Contexte

Sur la base du premier prototype macroscopique du transistor développé en 1947, des dispositifs microélectroniques sont apparus. En ouvrant la voie à de diverses et prometteuses applications, le domaine de la microélectronique est passé du monde académique à la production industrielle au début des années 1950. Depuis 1965, la loi de Moore a permis l'amélioration des techniques de fabrication des circuits électroniques, et également le développement de la technologie CMOS. En conséquence, les puces électroniques contiennent de plus en plus de transistors eux-mêmes de plus en plus petits année après année. Cette tendance est cependant confrontée à des limites physiques et économiques puisque les dimensions des transistors ne peuvent pas être réduites indéfiniment. Bien que leur production soit possible (mais chère), leurs caractéristiques électriques appartiennent au régime quantique rendant impossible toute utilisation de ces dispositifs dans les applications actuelles. Cependant, d'autres stratégies ont été développées permettant de nouvelles possibilités et de nouvelles applications (présentées dans la Figure I.1.1). L'approche «More than Moore » propose d'intégrer d'autres fonctionnalités dans les puces électroniques telles que les capteurs. Faites communément avec du silicium et avec d'autres matériaux de base de la technologie CMOS, ces structures mécaniques utilisent la même technologie de fabrication que les circuits électroniques.

Profitant de la production à faible coût, de la possibilité d'intégration à très grande échelle et de la compatibilité avec la technologie CMOS, ces systèmes électromécaniques deviennent très intéressants pour l'industrie des semi-conducteurs, et plus particulièrement pour la fabrication des capteurs.

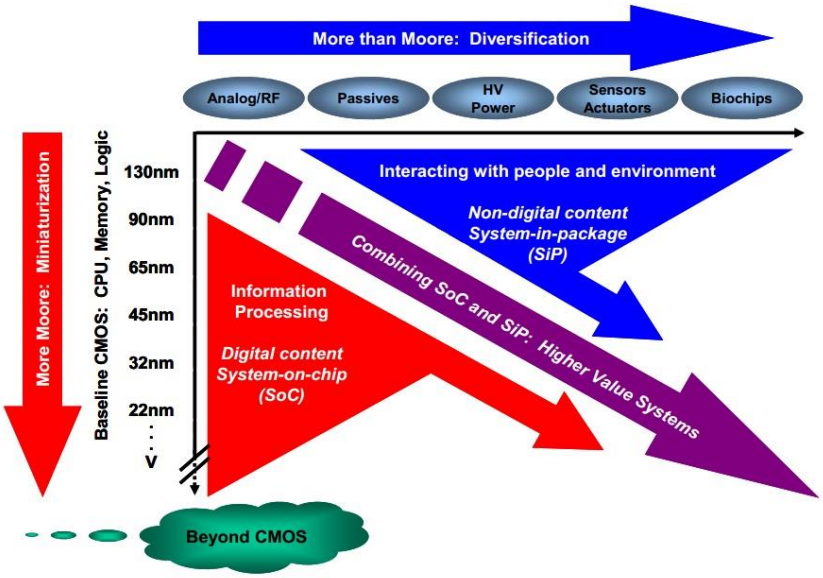
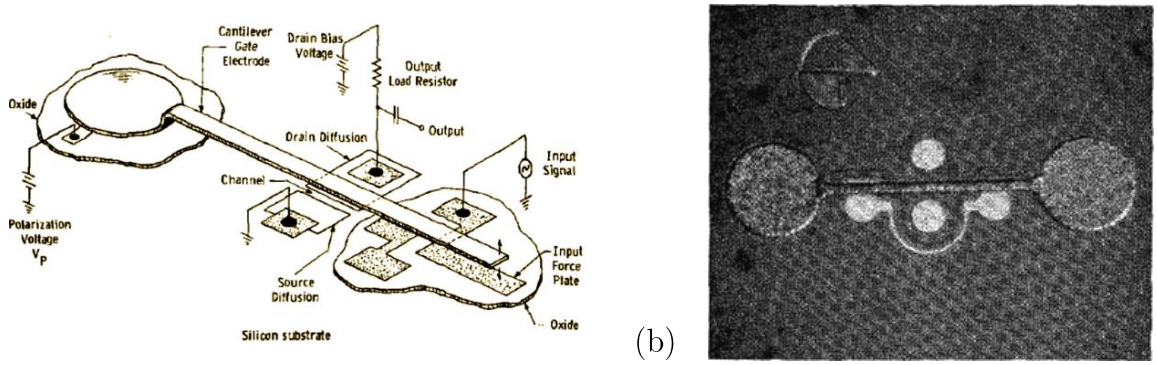


Figure I.1.1 : Représentation "More Moore vs More than Moore". Ce schéma montre les tendances technologiques majeures dispositifs microélectroniques et des microsystèmes [ITR10].

I.2 Historique

Développé en 1965 par l'équipe de Mr Nathanson, le transistor à grille résonante est considéré comme le premier système électromécanique utilisant des techniques de micro-usinage de surface [Nat65]. Ce dispositif (présenté en Figure I.1.2) a été construit en or. Cependant, le terme de microsystème électromécanique (MEMS) ne sera introduit que vingt-un ans plus tard par l'Agence pour les projets de recherche avancée de défense (DARPA), une agence du ministère américain de la Défense, en charge du développement de nouvelles technologies à des fins militaires [DAR].



(a) (b)

Figure I.1.2: Premier prototype de MEMS: le transistor à grille résonante. En (a) est présentée une description schématique d'un cantilever encastré-libre, (b) correspond à une photographie d'une structure encastrée-encastrée [Nat67].

Depuis le milieu du XX^{e} siècle jusqu'à nos jours, plusieurs évènements majeurs ont rendu omniprésente l'utilisation des MEMS dans notre vie quotidienne. En effet, la découverte et l'amélioration des techniques de fabrication, la transition des procédés de micro-usinage de volume vers les procédés de micro-usinage de surface, la création de fonderies et de procédés MEMS, la compatibilité avec la technologie CMOS, les premiers systèmes MEMS – CMOS co-intégrés et la miniaturisation des MEMS vers les NEMS ont rendu essentielle l'utilisation de ces dispositifs essentielle pour de nombreuses applications.

I.3 MEMS vs NEMS

L'architecture de tout système à base de M/NEMS est commune à de nombreux types de capteurs. L'élément central consiste en un seul voire plusieurs éléments mobiles organisés en matrice et en interaction avec leur environnement physique. Cette interaction peut prendre plusieurs formes: accélération, particules, irradiation de lumière, exposition de champ magnétique et électrique etc. Son mouvement est ensuite mesuré par un élément de détection électromécanique qui convertit le mouvement mécanique en un signal électrique. Ce signal peut ensuite être analysé par un circuit électronique (Figure I.1.3). Ces dispositifs MEMS peuvent être présents sous différentes formes (micro-capteurs, ASIC et micro-actionneurs) en fonction de l'application, comme décrit dans les Figures I.1.4 et I.1.5.

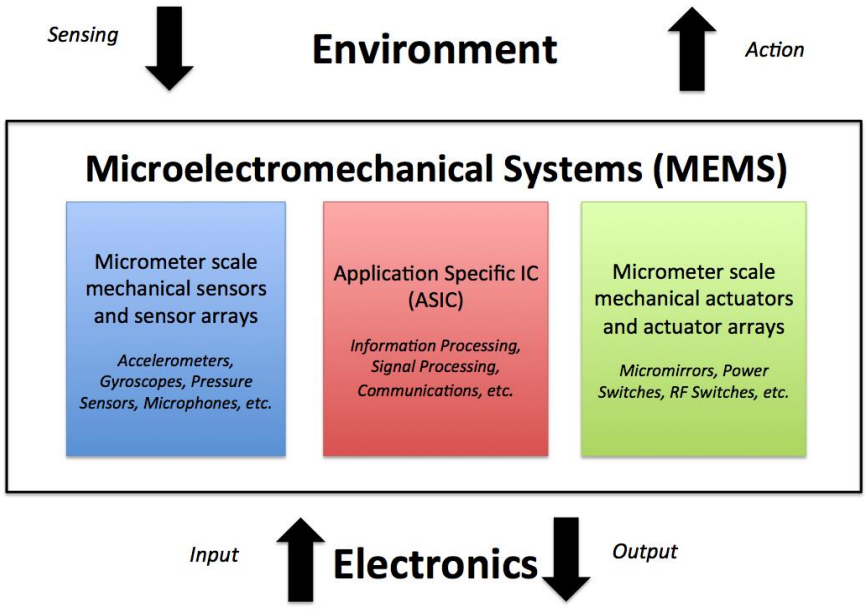


Figure I.1.3: Diagramme de fonctionnalité d'un composant MEMS [ITR13].

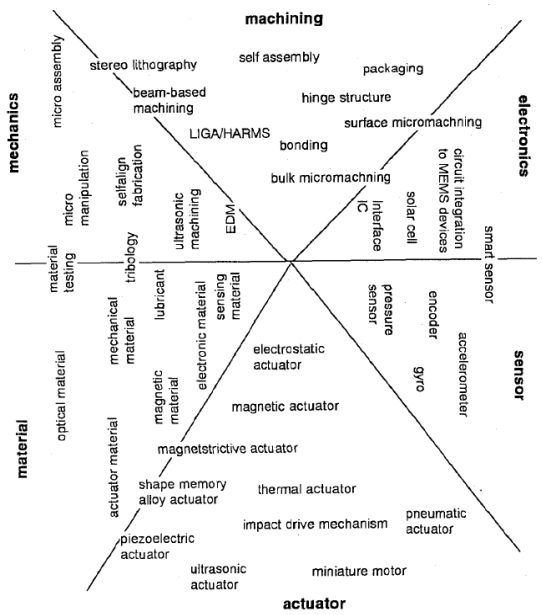


Figure I.1.4: Un large panel de dispositif MEMS... [Fuj97]

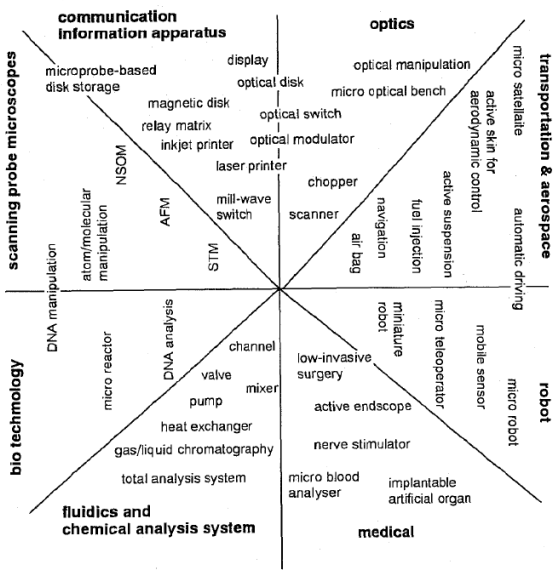


Figure I.1.5: ... pour une large variété d'application [Fuj97].

Résultat de la miniaturisation des dispositifs électromécaniques, les NEMS constituent de nouveaux objets innovants et diffèrent fortement des MEMS puisqu'ils n'adressent pas les mêmes applications. Effectivement, les MEMS sont de manière générale utilisés en tant que masse sismique pour les capteurs inertiels, tels que les accéléromètres [Lem11], gyroscopes [Wal12] et magnétomètres [Ett11]. Ces systèmes sont sensibles aux forces d'inertie en raison de leur masse, contrairement aux dispositifs NEMS. Grâce à leurs dimensions et à leurs faibles masses, ces derniers sont suffisamment sensibles pour détecter les minuscules changements dans leur environnement, comme les variations de concentration de particules ou de contraintes mécaniques. Les dimensions typiques des M/NEMS sont données en Figure I.1.6

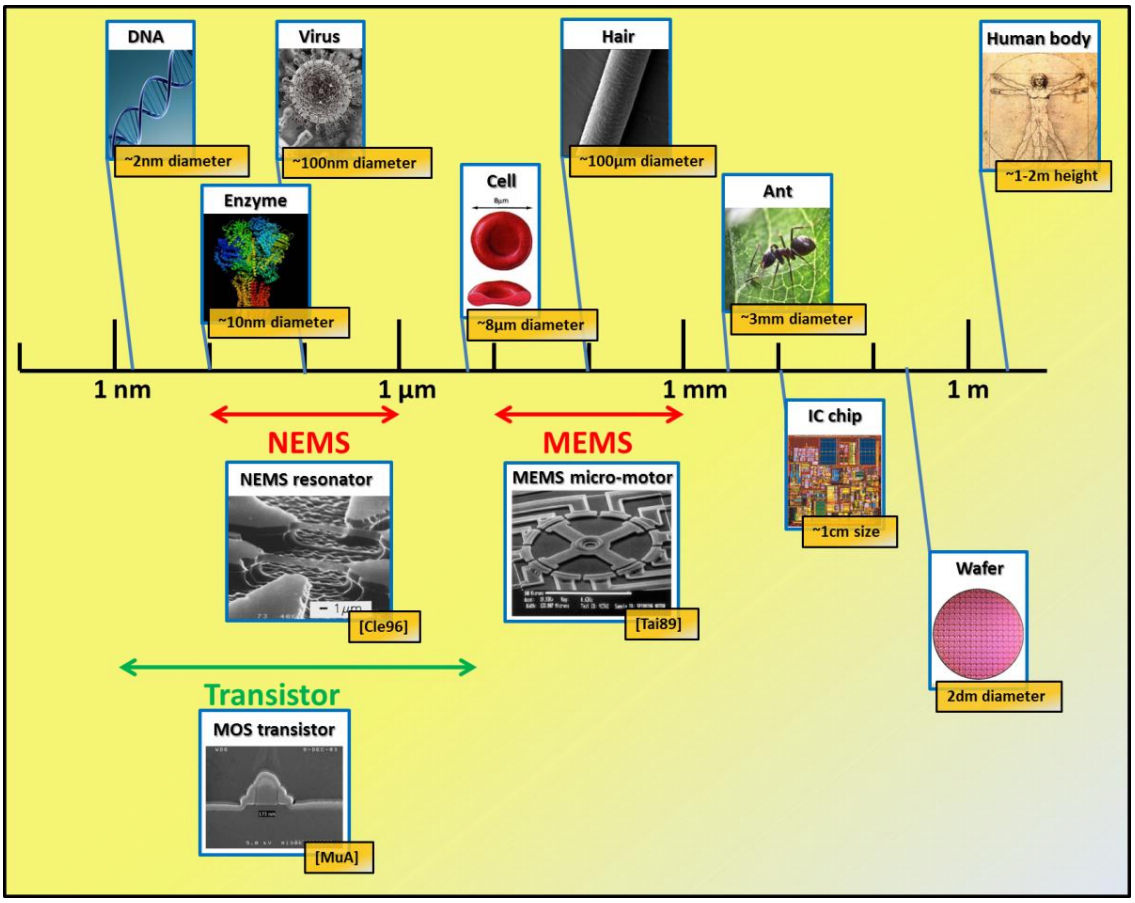
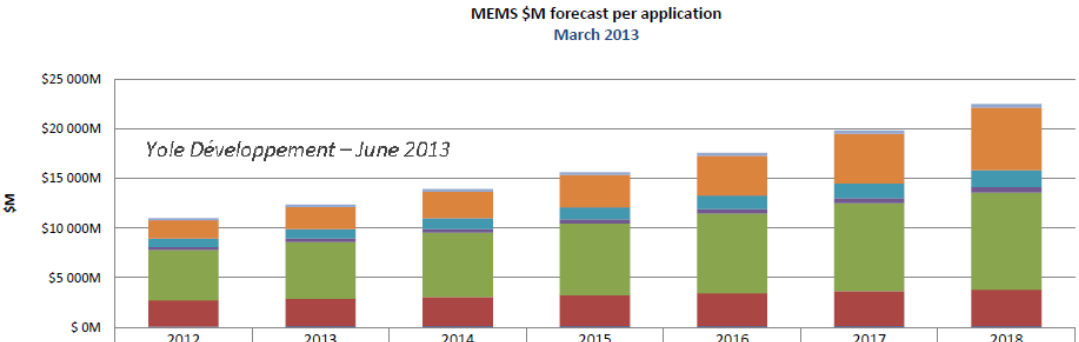


Figure I.1.6. Diagramme comparatif des dimensions pour les systèmes biologiques (en haut) et microélectroniques (en bas).

I.4 A propos du marché

Comme le montre la Figure I.1.7, le marché des MEMS est en constante croissance et devrait continuer à augmenter dans les années futures. Deux secteurs sont particulièrement concernés : l'automobile et la grande consommation (tels que les tablettes, smartphones, jeux vidéo, etc). Deux exemples typiques sont représentés dans la Figure I.1.8. Grâce à l'utilisation d'accéléromètres MEMS, Nintendo avec la Wii et Apple avec l'iPhone ont introduit l'utilisation de MEMS dans notre vie quotidienne et ont considérablement augmenté leurs chiffres d'affaires.

Les nano-systèmes électromécaniques sont encore au stade de développement et commencent à être commercialisés petit à petit. Ces systèmes pourraient entraîner l'émergence d'un nouveau type d'application nécessitant une haute sensibilité et un niveau de résolution, comme la détection de masse.



	2012	2013	2014	2015	2016	2017	2018
Telecom	$ 188M	$ 210M	$ 239M	$ 265M	$ 297M	$ 329M	$ 364M
Medical	$1 835M	$2 205M	$2 688M	$3 277M	$4 021M	$4 981M	$6 304M
Industrial	$ 874M	$ 963M	$1 069M	$1 203M	$1 339M	$1 495M	$1 676M
Defense	$ 297M	$ 335M	$ 379M	$ 421M	$ 470M	$ 525M	$ 583M
Consumer	$5 048M	$5 752M	$6 487M	$7 216M	$7 999M	$8 833M	$9 776M
Automotive	$2 639M	$2 760M	$2 934M	$3 115M	$3 322M	$3 503M	$3 643M
Aeronautics	$ 107M	$ 115M	$ 124M	$ 134M	$ 143M	$ 152M	$ 156M

Figure I.1.7: Diagramme illustrant la croissance du marché des MEMS dans différents segments. Source: Yole Development Status of MEMS Industry 2013.

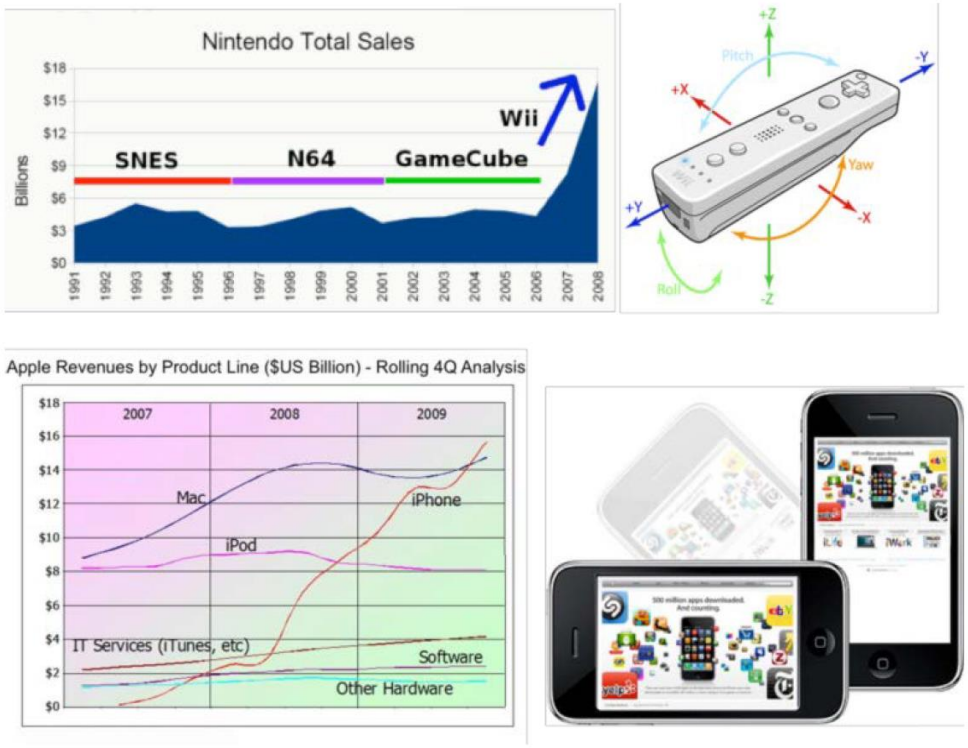


Figure I.1.8: Illustration de l'impact des MEMS dans les produits de consommation. Le chiffre d'affaires de Nintendo a fortement augmenté grâce à la commercialisation de la *Wii*, console utilisant la technologie MEMS pour la fabrication d'accéléromètres (en haut). Le chiffre d'affaire d'Apple a également fortement augmenté depuis l'année 2007, année correspondant à la commercialisation de l'*iPhone*. Ce produit utilise également des accéléromètres MEMS dans la technologie d'affichage (en bas) [ITR13].
Sources: http://www.straferight.com
http://www.osculator.net/
http://itcandor.net/2010/02/01/apple-results-q409/
http://askiphone.net/locking-your-iphone-screen-in-portrait-vertical-orientation/

II. Détecteur de masse à base de NEMS

II.1 Quelques exemples de détecteurs de masse courants

II.1.1 – Détection de gaz

Ce type de détecteur a pour objectif de déterminer la nature et la concentration de différentes espèces au sein d'un milieu gazeux. De nombreux exemples utilisant de multiples principes physiques peuvent être trouvés dans la littérature scientifique : les ISFETs [Ber70] et GasFETs [Lun75] qui utilisent l'effet de champ, les capteurs SAW [Woh79] et BAW [Jos02] utilisant les ondes acoustiques, les capteurs infrarouges [DET] etc. Certains de ces capteurs ne sont adaptés qu'à la détection d'une espèce particulière ou au contraire à plusieurs molécules au sein d'un gaz. Dans un cas, une étape de fonctionnalisation de la surface est nécessaire, dans un autre, une étape de chromatographie est requise pour la séparation des différentes espèces.

II.1.2 – Spectrométrie de masse

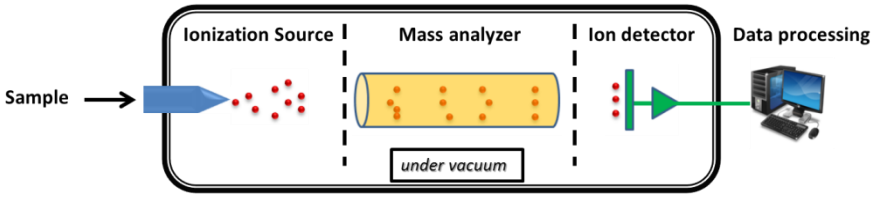


Figure I.2.1: Structure type d'un spectromètre de masse conventionnel.

La spectrométrie de masse est une technique universelle permettant de détecter la composition chimique d'un milieu liquide ou d'un gaz. Cette approche consiste à mesurer la trajectoire suivie par des particules chargées issues de l'ionisation d'un composé électriquement neutre à la base. Après la mesure, un analyseur de spectre est utilisé pour déterminer la nature de chaque espèce présente dans le mélange initial.

Cette méthode est très employée dans différentes branches scientifiques telles que la médecine, la biologie, la pharmacologie, la science des matériaux, la chimie, la géologie, et tend notamment à être utilisée dans le domaine de la protéomique pour l'analyse des biomolécules comme les protéines, les virus ou les bactéries.

La Figure I.2.2 montre que la spectrométrie de masse est capable de mesurer la quantité de particules de faible masse jusqu'à une valeur de 100kDa (kilo Dalton[16]). Cette valeur correspond typiquement à la masse de ces biomolécules. En raison de difficultés techniques (fort champ électromagnétique), de la faible résolution pour ces masses et de la perte d'information due à la destruction partielle des particules, cette technique conventionnelle n'est pas adaptée pour le domaine de la protéomique. L'utilisation de dispositifs à base de NEMS permet de résoudre les problèmes liés à la détection de biomolécules et à la mesure de composés neutres sans étape d'ionisation [Sag13].

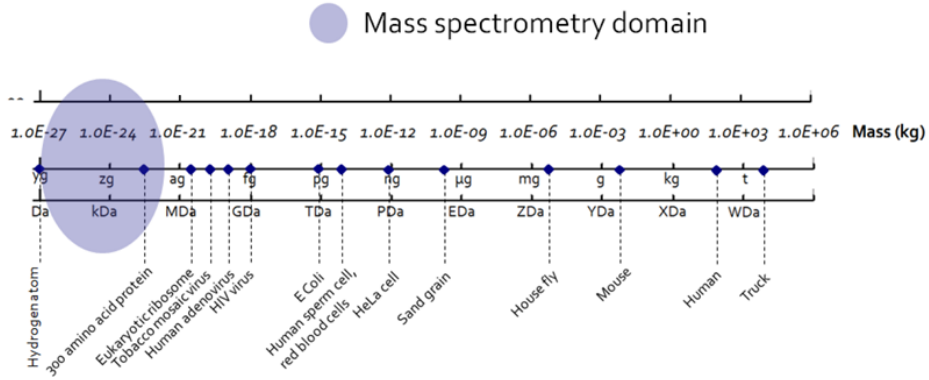


Figure I.2.2: Ordre de grandeur des masses détectées par la technique de spectrométrie de masse conventionnelle [Hen12].

II.2 La détection de masse à base de résonateurs NEMS

Le principe de détection de masse à base de résonateurs NEMS repose sur la mise en oscillation de ce résonateur, et particulièrement sur l'étude de la variation de la fréquence de résonance de la structure. Ce dispositif électromécanique peut être modélisé par un système masse-ressort. La fréquence de résonance f_0 du résonateur est donnée par la relation (I.1) dans laquelle M correspond à la masse totale du système et k à la constante de raideur du ressort.

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{M}} \qquad \text{(I.1)}$$

[16] Le Dalton (ou Da) est une unité de mesure utilisée pour la détection de masse. Un Dalton correspond à la masse d'un proton, c'est-à-dire $1.67.10^{-27}$g.

Si une petite masse Δm (en comparaison avec la masse du système mécanique) est adsorbée à la surface du résonateur, un décalage de la fréquence de résonance apparaît, ce décalage Δf étant proportionnel à Δm comme indiqué en (I.2).

$$\Delta f \approx \frac{\Delta m}{2M} \cdot f_0 \tag{I.2}$$

Ainsi, en mesurant l'évolution de cette fréquence de résonance, le résonateur NEMS peut être utilisé en tant que détecteur de masse, comme montré en Figure I.2.3.

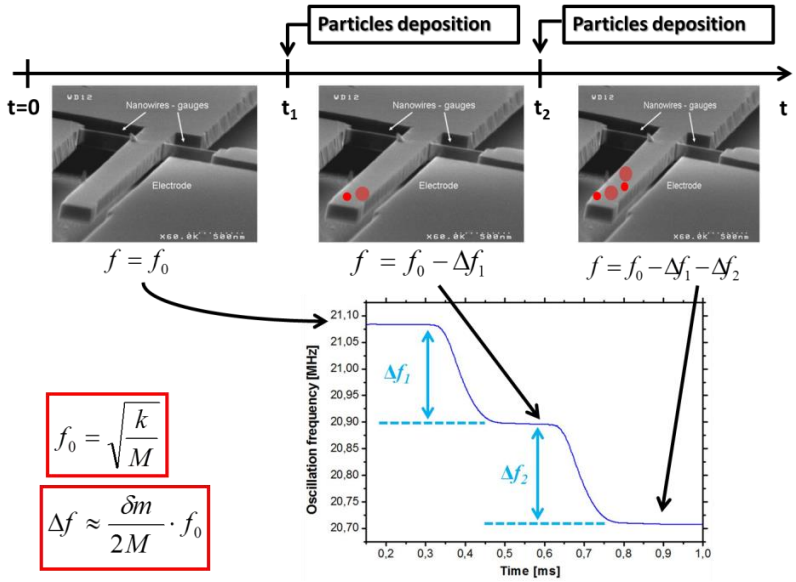


Figure I.2.3: Illustration schématique de l'utilisation d'un résonateur NEMS en tant que détecteur de masse. L'évolution de la fréquence de résonance au cours du temps est étudiée. Chaque variation de fréquence est directement proportionnelle à la masse adsorbée par la structure.

Deux critères majeurs caractérisent la performance de détection d'un capteur de masse : la sensibilité et la résolution massique. La sensibilité R correspond à la variation de la fréquence de résonance f_0 en fonction de la masse m déposée sur le résonateur (dans le cas de capteurs à base de NEMS). Cette caractéristique montre comment le système réagit lorsqu'il subit une légère perturbation. La résolution massique *óm* constitue par définition la plus petite masse que peut détecter le capteur. Les équations (I.3) et (I.4) définissent ces deux notions et montrent que R et *óm* dépendent de la fréquence de résonance mécanique f_0, de la masse du résonateur M, du facteur de qualité Q, de la plage dynamique DR du capteur. Ces deux caractéristiques sont liées entre autre à la dimension du résonateur L.

$$R = -\frac{\partial f_0}{\partial m} = \frac{f_0}{2M} \propto L^{-4} \qquad [\mathrm{Hz.kg^{-1}}] \qquad \text{(I.3)}$$

$$\delta m = \frac{M}{Q} \cdot 10^{-\frac{DR}{20}} \propto L^3 \qquad [\mathrm{kg}] \qquad \text{(I.4)}$$

La description des capteurs de gaz et des spectromètres de masse faite précédemment permet de voir les critères les plus importants pour la constitution d'un détecteur de masse de haute performance :

- une miniaturisation facile à mettre en place nécessitant peu d'étapes de fabrication :
- une production à bas coût ;
- une faible consommation en énergie ;
- un temps de réponse rapide ;
- un haut niveau de sensibilité ;
- et une faible résolution ;

Les résonateurs M/NEMS répondent parfaitement à ces critères. Ils contiennent trois éléments caractéristiques : une partie mobile (généralement une poutre), un étage d'actionnement et un étage de détection. La partie mobile constitue l'élément sensitif et est mis en mouvement par l'étage d'actionnement. L'étage de détection quant à lui convertit le déplacement mécanique de la partie mobile en une tension électrique dont l'information peut être traitée par un circuit électronique. De tels dispositifs sont couramment fabriqués en suivant une approche dite « top-down » nécessitant des procédés d'usinage en volume et/ou en surface.

La littérature reporte des exemples de fabrication de capteurs utilisant des résonateurs M/NEMS [Lan02 – Arc11], ainsi que les premières déterminations de résolution massique de résonateurs NEMS [Eki04 - Cha12] et la première démonstration expérimentale d'un spectromètre de masse à base de résonateur NEMS [Nai09].

II.3 Contraintes de l'implémentation de résonateurs M/NEMS pour la détection de masse

Comme décrit précédemment, un haut niveau de sensibilité et une faible résolution massique sont nécessaires à la fabrication de détecteur de masse de haute performance. D'après les équations (I.3) et (I.4), R et *óm* étant reliées à la dimension du résonateur L, une miniaturisation de la structure permettrait d'augmenter de manière conséquente les performances du détecteur comme décrite dans la Figure I.2.4. Cette tendance est illustrée dans le Tableau I.1.

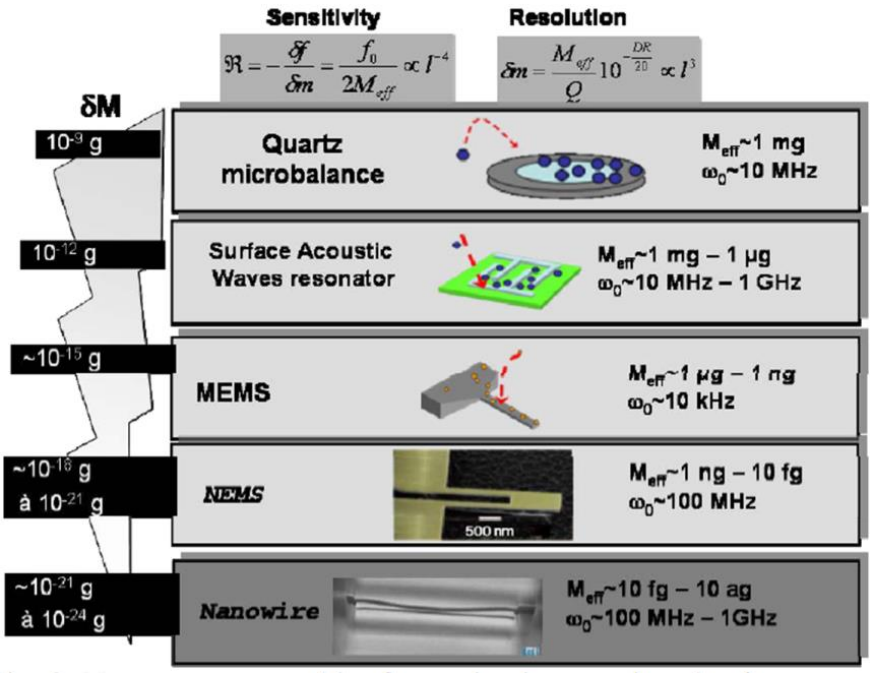


Figure I.2.4: Variation de la fréquence de résonance et de la résolution massique en fonction de la miniaturisation du système électromécanique.

Références	**[Eki04]**	**[Yan06]**	**[Chi08]**	**[Cha12]**
L (µm)	10	2.3	0.4	0.150
f_0 (MHz)	72	133	300	1862
R (MHz/pg[17])	2.56	890	$9.3x10^7$	$3.1x10^{12}$
δm (ag[18])	2.53	$7x10^{-3}$	$85x10^{-6}$	$1.7x10^{-6}$

Tableau I.1: Amélioration de la sensibilité et de la résolution massique grâce à la miniaturisation du résonateur.

[17] Un picogramme (ou pg) est égal à 1.10^{-12}g.

[18] Un attogramme (ou ag) est égal à 1.10^{-18}g.

Par conséquent, une transition des MEMS vers les NEMS est nécessaire pour produire des détecteurs de haute performance. L'utilisation de ces nano-systèmes requiert une grande présence de ces derniers disposés au sein d'un réseau (comme montré à la Figure I.2.5) afin d'augmenter la surface de capture et de collecter un maximum de particules collectées.

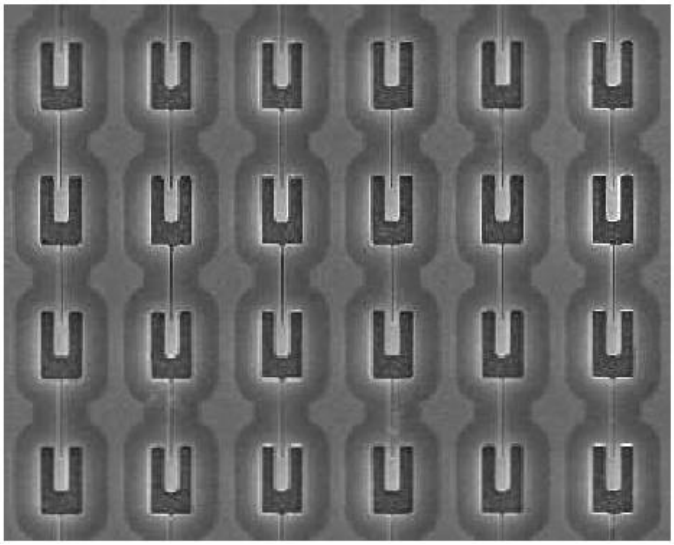
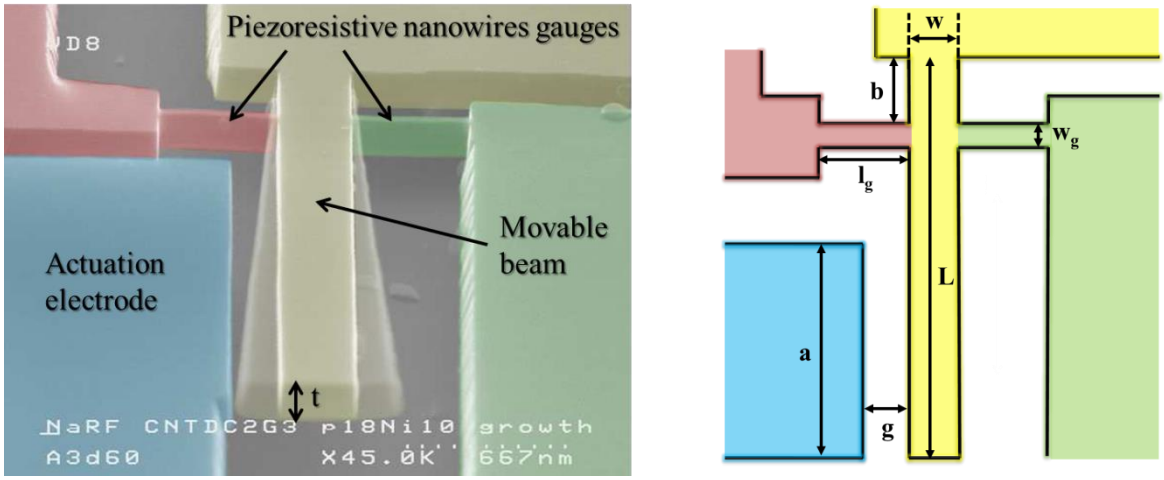


Figure I.2.5: Exemple de résonateurs NEMS arrangés au sein d'une matrice [Arl11].

Cette miniaturisation pose en revanche quelques contraintes. La réduction de taille entraîne la réduction du déplacement du cantilever qui devient en conséquence très difficile à détecter. Le principe utilisé pour la détection devient donc un enjeu crucial pour l'utilisation des NEMS dans la détection de masse. Une architecture bien adaptée pour cette application consiste à fabriquer les résonateurs en silicium monocristallin (c-Si) en utilisant la zone active d'un substrat SOI, et à utiliser un actionnement électrostatique combiné à une détection piézorésistive. Cette structure appelée « crossbeam » est illustrée en Figure I.2.6 [Mil10]. Le c-Si constitue un excellent matériau puisqu'il possède un très fort facteur de jauge piézorésistif [Bar09]. De plus, l'utilisation de ce matériau permet une production à très grande échelle et à bas coût, avec une possibilité de co-intégration avec un circuit CMOS.



Beam length	Beam width	Gap electrode/beam	Gauge length	Gauge width	Electrode length	Anchor/gauge distance	Beam thickness
L	W	g	l_g	w_g	a	b	t
~5µm	~300nm	~200nm	~500nm	~80nm	~3.5µm	~750nm	~160nm

Figure I.2.6: Image MEB modifiée et colorée artificiellement illustrant une structure “crossbeam” (sur la gauche) [Mil10] et présentation de ses dimensions géométriques (sur la droite). Le tableau en dessous indique les valeurs typiques de celles-ci. La miniaturisation de la structure peut s’appliquer sur tous ces paramètres géométriques.

III. Intégration M/NEMS-CMOS

L'utilisation de résonateurs M/NEMS pour les applications de détection de masse nécessite la mise en oscillation du système et la détection de toute variation de la fréquence d'oscillation. Ces conditions imposent une configuration en boucle fermée du système ainsi qu'un circuit électronique pouvant être fabriqué en technologie CMOS. Le circuit permet non seulement de mettre le résonateur en oscillation, mais également de lire et de traiter le signal en sortie du système électromécanique. L'intégration M/NEMS-CMOS constitue un point crucial pour la fabrication de capteur de masse, plus particulièrement la méthode pour interconnecter la partie M/NEMS avec la partie CMOS. Deux stratégies d'intégration principales existent : l'approche dite hybride et l'approche dite monolithique (voir Figure I.3.1).

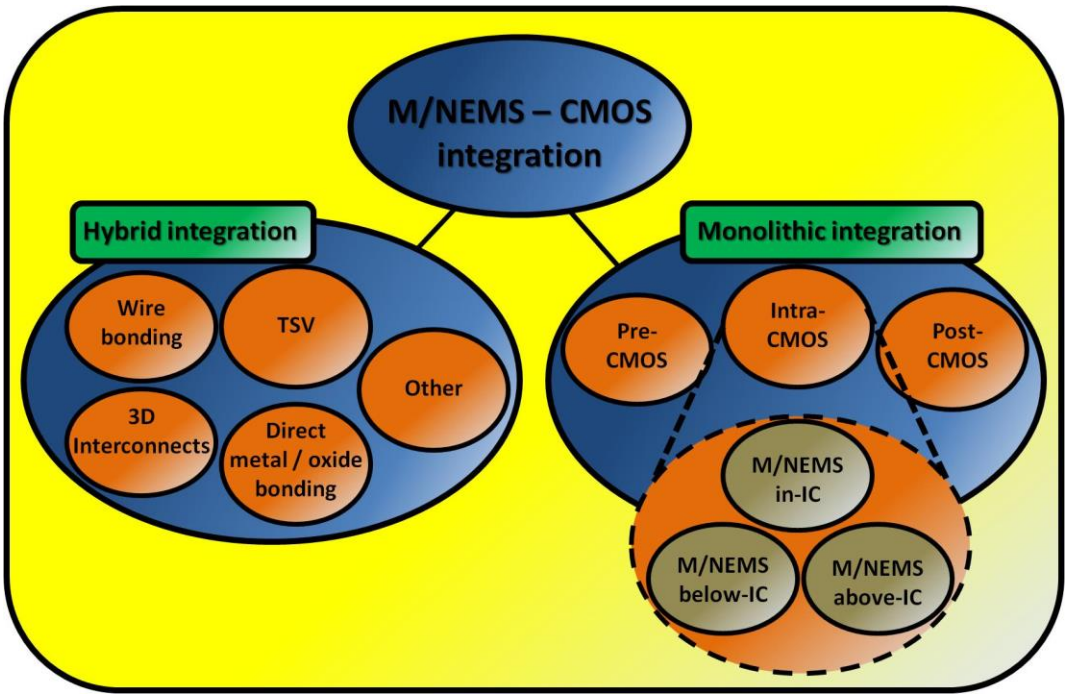


Figure I.3.1: Diagramme représentant différentes technologies d'intégration M/NEMS-CMOS.

III.1 L'intégration hybride (dite parallèle ou « stand-alone »)

Cette approche consiste à fabriquer différentes fonctions (par exemple mémoire, module énergétique, MEMS, CPU etc) sur des puces séparées, de les assembler et connecter entre elles (voir Figure I.3.2) pour créer des puces multifonctionnelles. De cette manière, chaque élément peut être développé sans impacter la fabrication de l'autre. Différentes possibilités existent pour ce type d'approche : le câblage par fil ou pontage (« wire bonding » en anglais), l'utilisation d'interconnecteurs 3D, le collage direct métal-oxyde et l'utilisation de TSV.

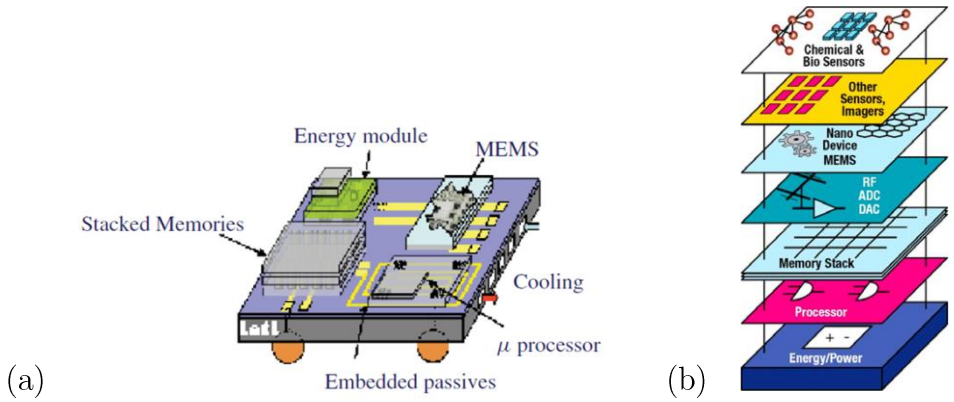


Figure I.3.2: Représentation d'une puce multifonctionnelle élaborée suivant une stratégie d'intégration hybride utilisant à la fois des approches 2D et 3D (a) [Sou11] et illustration d'une approche 3D présentant un exemple d'une « hyper intégration 3D » (b) [Lu09].

III.1.1 – Câblage par fil

Le câblage par fil est une technique classique qui consiste à interconnecter deux plots métalliques par un fil, comme illustré sur la Figure I.3.3. Cette technique présente de nombreux avantages : le procédé est compatible avec la technologie CMOS (température inférieure à la température maximale que peut subir le circuit électronique, généralement de 450°C), étape facile à réaliser (une seule étape et faibles contraintes d'alignement). L'inconvénient majeur de cette technique vient de la forte capacité parasite (jusqu'à 10pF [Arn11]) pouvant générer une forte atténuation du signal.

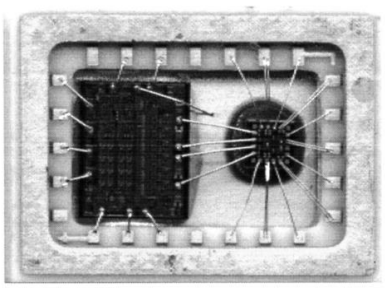
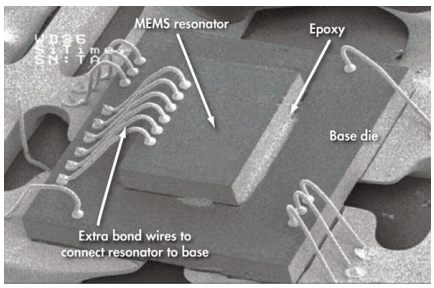
(a)  (b) 

Figure I.3.3: Câblage filaire réalisé en 2D entre une puce contenant un MEMS RF et un circuit CMOS (a) [Sil03] et exemple de câblage filaire réalisé en 3D (b) [Pet13]

III.1.2 – Interconnecteurs 3D pour assemblage avec puce retournée (ou "flip-chip")

Cette approche consiste à fabriquer des interconnecteurs sur une des deux puces pour ensuite les assembler (généralement via des techniques thermo-compressives). Différents types d'interconnecteurs peuvent être utilisés : des micro-inserts [Wat10], des micro-tubes [Mar13], des micro-bumps [Mil69-Che09], des interconnecteurs TLP (pour « Transient Liquid Phase ») [Col13] etc (voir Figure I.3.4). Plus de détails concernant leurs procédés de fabrication sont fournis dans [Lam13] et [Col13].

Contrairement au câblage filaire, l'assemblage via des interconnecteurs 3D ne souffre pas de capacités parasites, constituant un fort avantage. En revanche, cette stratégie nécessite de nombreuses étapes de fabrication et des contraintes d'alignement particulièrement fortes lors de l'assemblage, ainsi qu'un pas entre interconnecteurs élevé (10µm minimum) affectant la densité du réseau de résonateurs NEMS.

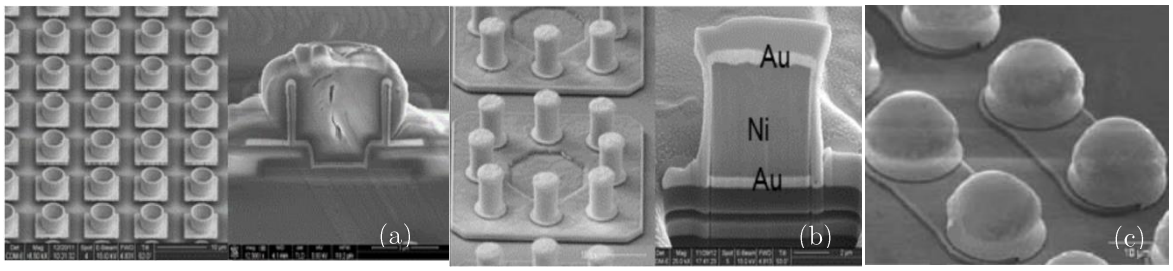


Figure I.3.4: Images MEB et FIB de micro-tubes (a) [Col13], micro-inserts (b) [Col13] et de micro-bumps (c) [Lau11].

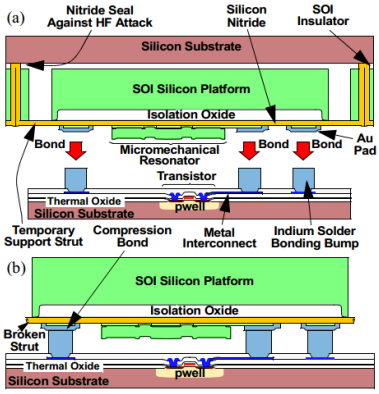


Figure I.3.5: (a) Vue schématique en coupe d'une integration 3D NEMS-CMOS via l'utilisation de micro-bumps (b) [Won01].

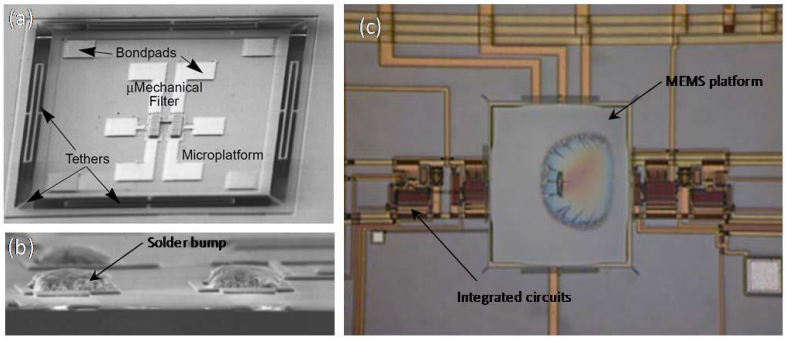


Figure I.3.6: Image MEB (a) montrant le dispositif électromécanique et ses plots métalliques associés. L'image (b) est un zoom sur les micro-bumps fabriqués sur la puce du circuit électronique. L'image (c) nous montre l'assemblage final avec la puce MEMS localisée sur la puce CMOS [Won01].

III.1.3 – Collage direct métal-oxyde

Le collage direct métal-oxyde est une technique permettant de coller et d'interconnecter deux substrats différents. Ce collage peut être réalisé de différentes manières (voir Figure I.3.7). Cette stratégie d'intégration est intéressante puisqu'elle permet de réaliser une intégration substrat à substrat contrairement à celle réalisée avec des interconnecteurs 3D. De plus, contrairement à l'approche précédente, le pas entre deux plots métalliques peut être réduit (<10µm [Bei13]) et permettre ainsi la fabrication d'un réseau dense de NEMS. D'autre part, la capacité parasite est faible. Cette technique nécessite cependant de fortes contraintes en terme de topologie de surface et d'alignement lors de l'assemblage.

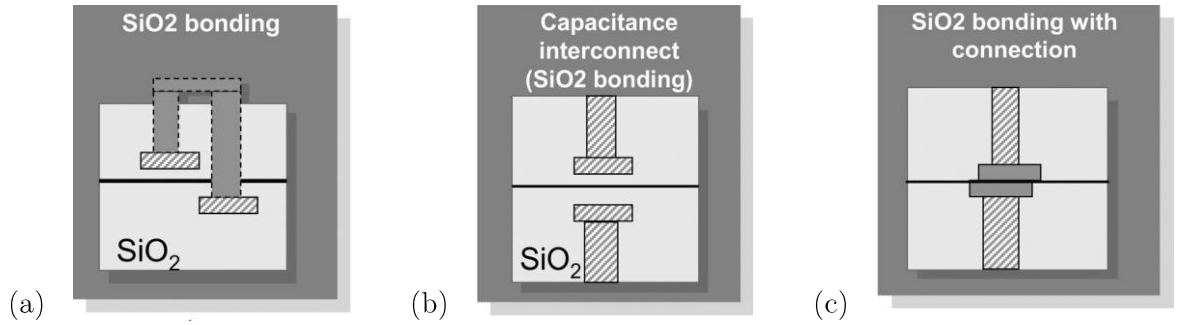


Figure I.3.7: Vue en coupe de différentes options pour l'intégration par collage direct: réalisation d'interconnexion résistive (a) ou capacitive (b), ou collage direct métal-oxyde (c). Les formes hachurées et sombres représentent les niveaux de métal [Cio11].

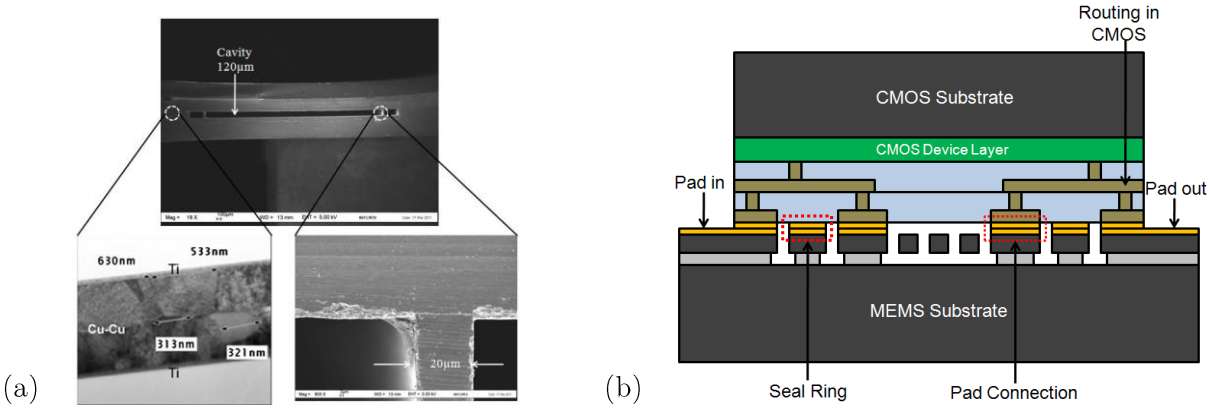


Figure I.3.8: Images MEB d'un collage Cu-Cu (a) et vue en coupe schématique d'un système MEMS-CMOS utilisant la technique de collage directe Cu-Cu (le Cu est représenté en jaune) (b) [Nap12].

III.1.4 – Intégration utilisant les Through Silicon Vias (TSV)

Les TSVs correspondent à de larges et longs vias métalliques verticaux utilisés pour l'intégration 3D et l'empilement de puces. Plusieurs stratégies de fabrication existent et sont exposées en Figure I.3.9.

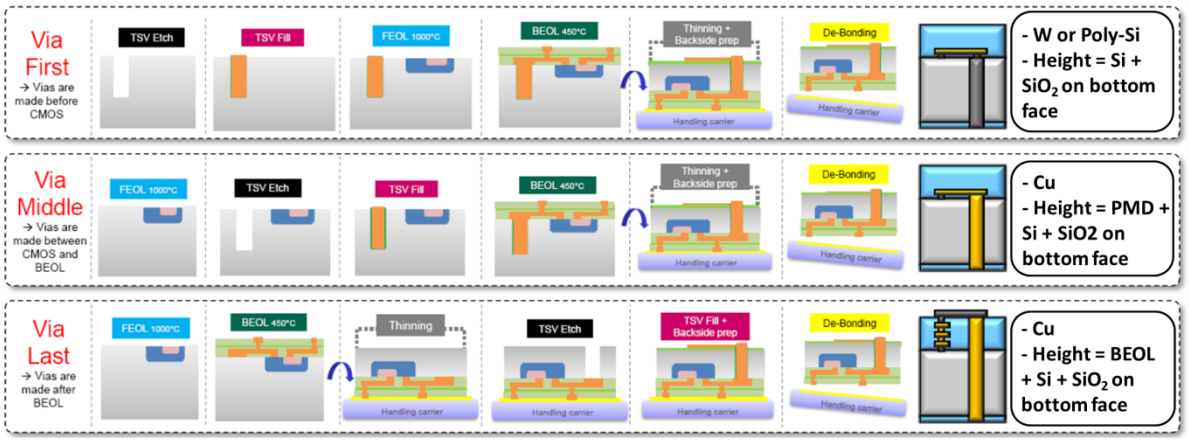


Figure I.3.9: Schéma montrant différentes possibilités d'intégration utilisant des TSVs [Bro2013].

L'utilisation de TSVs introduit de fortes capacités parasites (proches de 100fF [Cad11-Lee14]) pouvant entraîner de fortes atténuations de signal durant la transmission entre les dispositifs NEMS et le circuit CMOS. Un autre inconvénient de cette approche concerne le pas entre les TSVs qui ne peut être inférieur à 10µm (notamment à cause de la «Keep-out zone » [Ryu12]), limitant ainsi la densité des nano-résonateurs.

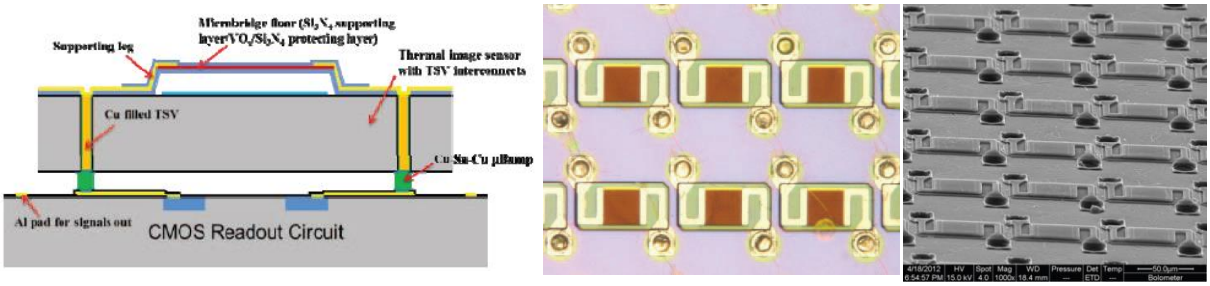


Figure I.3.10: Vue en coupe d'un capteur MEMS-CMOS interconnecté à l'aide de TSVs (à gauche) et image obtenue en microscopie optique et MEB du réseau de MEMS associé (respectivement au milieu et à droite) [Wan12].

III.2 Intégration monolithique

L'intégration monolithique consiste à fabriquer la partie M/NEMS et la partie CMOS sur la même puce.

III.2.1 –Description d'un empilement CMOS

Une puce CMOS est caractérisée par trois régions principales (illustrée en Figure I.3.11) :

- La zone front-end (notée FE) dans laquelle les dispositifs fonctionnels comme les transistors, les mémoires etc sont fabriqués ;
- La zone middle-end (notée ME) dans laquelle sont fabriqués les contacts pour les grilles des transistors et pouvant contenir des couches de slicium poly-cristallin ;
- La zone back-end (notée BE) contenant les interconnexions métalliques

La Figure I.3.11 indique non seulement les différents matériaux en présence dans chaque zone, mais également la température maximale que peut supporter chacune d'entre elle.

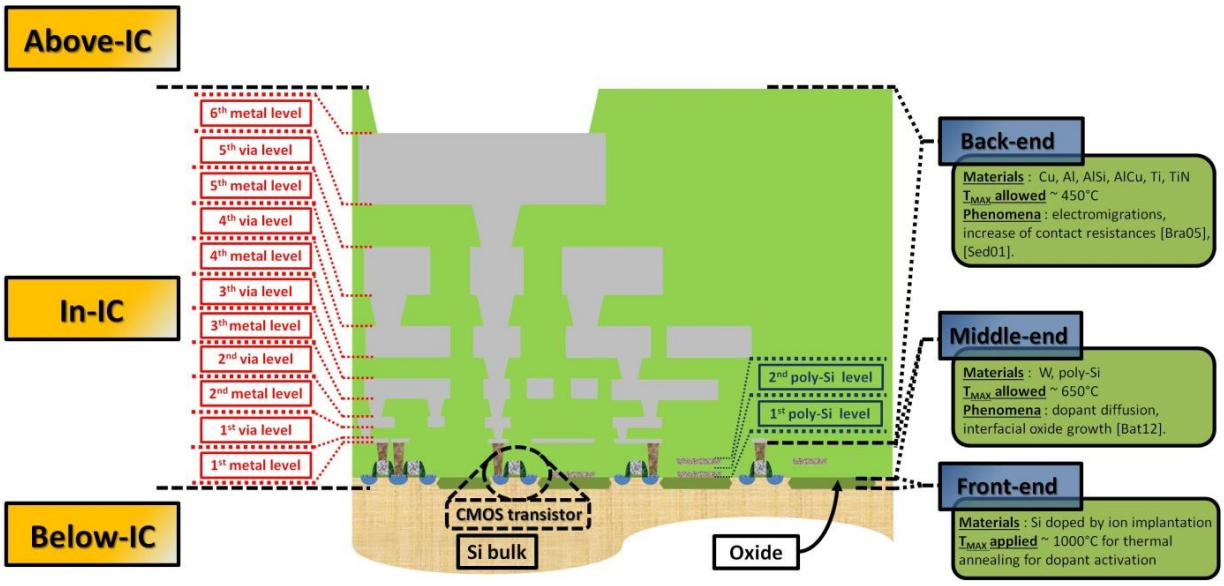


Figure I.3.11: Illustration d'une puce standard CMOS.

III.2.2 – Procédé de fabrication de résonateur M/NEMS

La Figure ci-dessous illustre un procédé de fabrication standard d'un résonateur NEMS fait en c-Si. Les conditions et les températures utilisées durant le processus sont importantes dans le but d'intégrer le NEMS avec le circuit CMOS afin de ne pas endommager ce dernier.

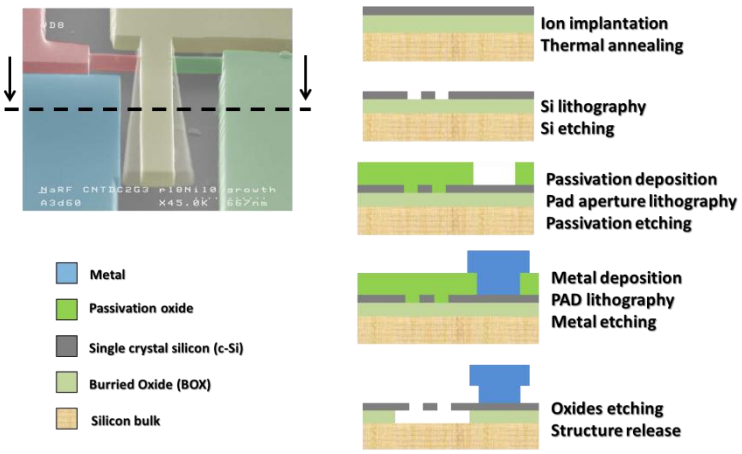


Figure I.3.12: Procédé de fabrication typique de résonateur NEMS.

III.2.3 – Position du résonateur M/NEMS au sein de l'empilement CMOS

Au sein d'un empilement CMOS, de nombreuses possibilités existent pour intégrer monolithiquement la partie NEMS par rapport à la partie CMOS.

- M/NEMS en dessous du circuit CMOS (M/NEMS below-IC)

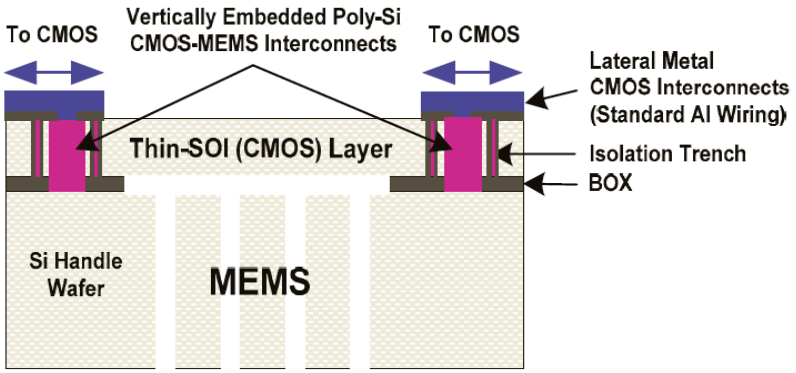


Figure I.3.13: Schéma d'un NEMS en dessous d'un circuit CMOS [Raj12].

- M/NEMS au niveau du circuit CMOS (M/NEMS in-IC)
  - au niveau du front-end (M/NEMS in FE) ;

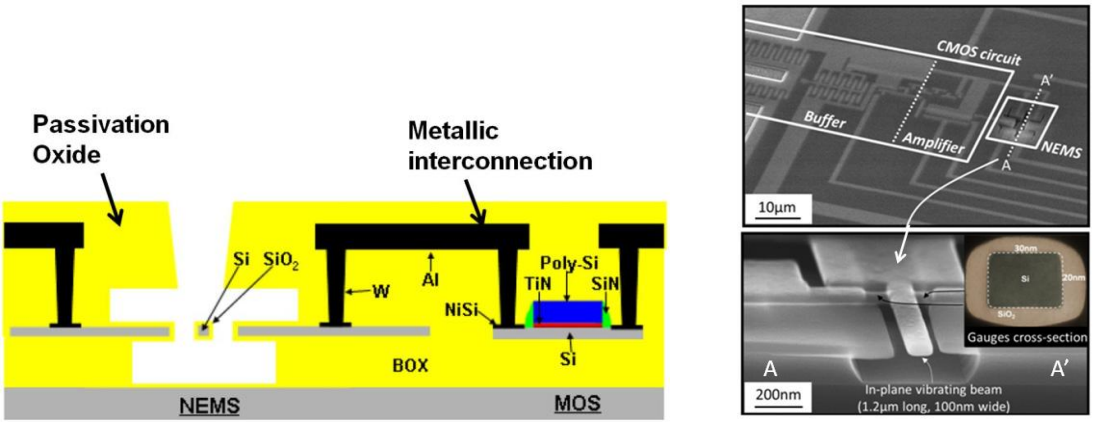


Figure I.3.14: Vue schématique en coupe (à gauche) et image MEB (à droite) d'un NEMS réalisé au niveau front-end et co-intégré avec un circuit CMOS réalisé en technologie FDSOI [Oll12].

- au niveau du middle-end (M/NEMS in ME);

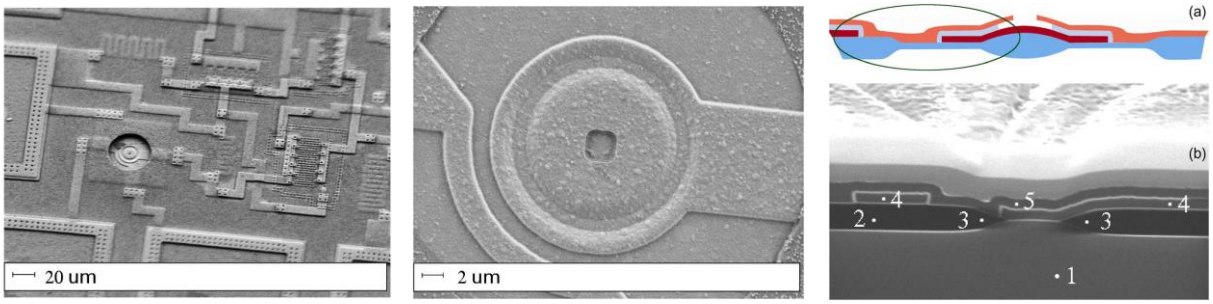


Figure I.3.15: Image MEB d'un système MEMS-CMOS (à gauche) avec un zoom sur le dôme résonant (au milieu) et sa vue schématique en coupe (a) et réelle (b) [Zal10]. Sur l'image MEB à droite sont indiquées les différentes couches de la structure : (1) correspond au substrat de silicium, (2) et (3) à des oxydes, (4) et (5) respectivement aux premières et secondes couches de silicium poly-cristallin.

- au niveau du back-end (M/NEMS in BE);

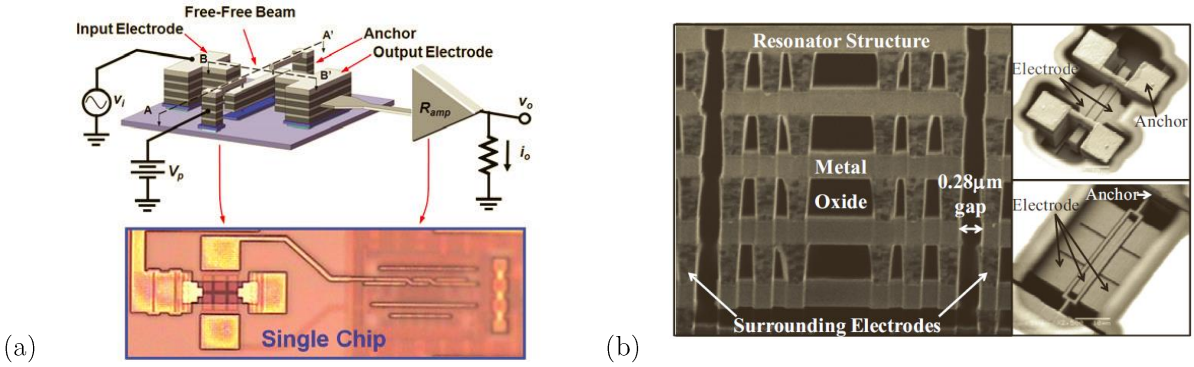


Figure I.3.16: Présentation d'un dispositif MEMS-CMOS utilisant toutes les interconnexions métalliques comme couche structurale du MEMS. En (a) est montré un schéma et une image par microscopie optique du système. Une vue de dessus et en coupe faite au MEB de différentes structures résonantes sont présentées en (b).

- M/NEMS au-dessus du circuit et des interconnexions (M/NEMS above-IC)

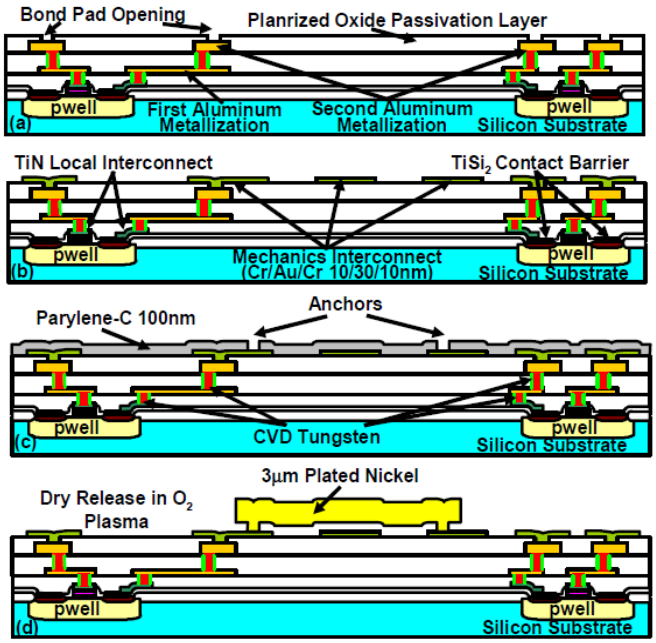


Figure I.3.17: Schéma en coupe d'un système MEMS-CMOS avec un MEMS réalisé en Ni au-dessus des interconnexions [Hua08].

IV. Discussion et conclusion

Ce chapitre a permis de voir l'intérêt des résonateurs NEMS pour les applications de détection de masse. L'utilisation de ces systèmes électromécaniques implique d'une part la fabrication d'un grand réseau de ces objets ainsi qu'un circuit électronique jouant le rôle de système de rebouclage. Cette intégration entre NEMS et CMOS doit respecter certaines spécificités pour constituer un détecteur de masse performant, comme :

- Une faible capacité parasite afin de diminuer l'atténuation de signal entre l'élément mécanique et le circuit électronique ;
- Une forte densité de NEMS en surface pour augmenter la surface de capture ;
- Une faible consommation de surface de la part du capteur ;
- Un procédé de fabrication simple et à bas coût.

L'intégration monolithique apparaît comme une solution prometteuse puisqu'elle permet de satisfaire tous ces critères. Dans le but de profiter des propriétés électromécaniques du c-Si, deux stratégies d'intégration monolithique peuvent être utilisées : une intégration dans laquelle le NEMS est fabriqué au niveau du FE et une autre dans laquelle le NEMS se situe au-dessus du circuit et des interconnexions. Ces deux stratégies seront davantage étudiées dans les deux prochains chapitres.

Chapitre II

Démonstration expérimentale d'un dispositif NEMS-CMOS co-intégré en 2D

Dans ce chapitre sera étudié un exemple de réalisation de système NEMS-CMOS utilisant une intégration monolithique dans laquelle l'élément électromécanique est réalisé dans la zone front-end et à côté du circuit électronique. Les résultats électriques de ce dispositif seront étudiés et une modélisation de ce système permettant de comprendre son fonctionnement sera exposée, le but final étant la création d'un auto-oscillateur NEMS-CMOS.

I. Modélisation du système NEMS-CMOS

Cette section se propose de décrire le système NEMS-CMOS du point de vue modélisation. Le dispositif électromécanique étudié dans ce chapitre (illustré en Figure II.1.1) utilise un actionnement électrostatique et une détection capacitive.

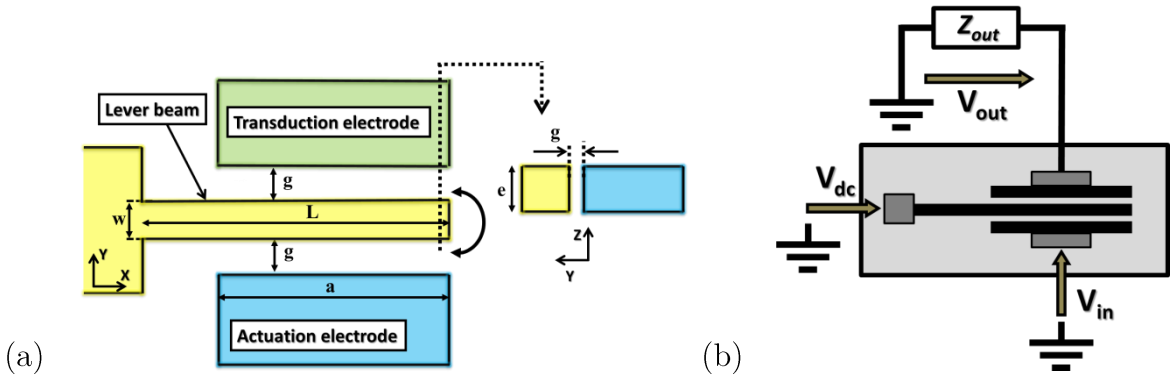


Figure II.1.1: Représentation schématique (a) et montage électrique (b) d'un résonateur NEMS à trois ports composé d'une poutre encastrée-libre.

I.1 Description du dispositif et modèle électromécanique

Comme décrit dans le chapitre précédent, le résonateur NEMS comprend trois étages différents : une partie actionnement, un élément résonant et une partie détection. Le système peut être décrit sous forme de schéma bloc comme indiqué en Figure II.1.2. Chacun de ces blocs est caractérisé par sa fonction de transfert.

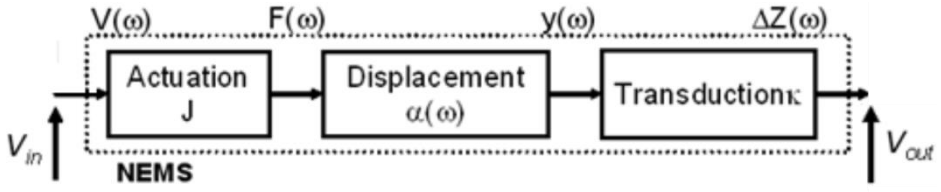


Figure II.1.2: Schéma bloc d'un résonateur [Col09].

I.1.1 – Actionnement

L'actionnement a pour but de mettre en mouvement une structure libre (une poutre par exemple). Cet étage convertit un signal d'entrée V_{in} qui peut avoir des origines diverses (optique, magnétique, thermoélastique etc) en une force F agissant sur la structure. Dans notre cas, cet actionnement convertit une tension électrique en une force électrostatique. Il est caractérisé par un gain J correspondant au ratio entre la force résultante et la tension d'entrée, comme indiqué en (II.1).

$$J = \frac{F(\omega)}{V_{in}(\omega)} = \frac{\varepsilon_0 ea}{g^2} V_{dc} \ [\mathrm{N.V^{-1}}] \tag{II.1}$$

I.1.2 – Dynamique du NEMS

La fonction de transfert $\alpha(\omega)$ entre la force d'actionnement et le déplacement résultant de la poutre peut être obtenue grâce à l'équation d'Euler-Bernouilli pouvant être résolue grâce à la procédure de Galerkin[19]. Une autre méthode consiste à modéliser le résonateur comme un système masse-ressort caractérisé par une masse m (en kg), une constante de raideur k (en $\mathrm{N.m^{-1}}$), un coefficient d'amortissement c ($\mathrm{N.m^{-2}}$) et sur lequel une force F_{act} (électrostatique ici) est appliquée, comme illustré en Figure II.1.3.

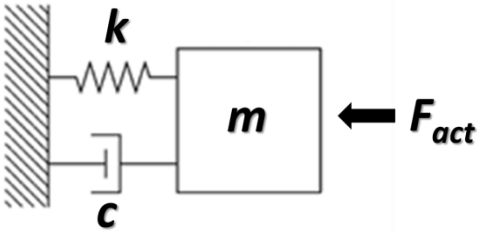


Figure II.1.3: Système masse-ressort amorti utilisé pour modéliser le résonateur.

En supposant que les déplacements de la poutre sont très faibles comparés à une amplitude critique [Mil10-Kac09], le système peut être considéré comme linéaire. De ce fait, le second principe fondamental de la dynamique permet d'obtenir la relation (II.2):

$$\alpha(\omega) = \frac{y(\omega)}{F_{act}(\omega)} = \frac{1}{-m\omega^2 + jc\omega + k} = \frac{\frac{1}{k}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \ [\mathrm{m.N^{-1}}] \tag{II.2}$$

[19] Plus d'informations sont en [Arn11] et [Mil10].

$$\text{avec } \omega_0 = \sqrt{\frac{k}{m}} \text{ [rad.s}^{-1}\text{]} \tag{II.3}$$

$$\text{et } Q = \frac{\sqrt{k \cdot m}}{c} \tag{II.4}$$

ω_0 and Q correspondent respectivement à la pulsation de résonance mécanique du premier mode et au facteur de qualité propre à ce mode de résonance. En suivant l'approche d'Euler-Bernouilli, la pulsation de résonance, la constante de raideur effective et la masse effective de la structure peuvent être calculées selon la dimension de la poutre et les propriétés du matériau le constituant [Arn11].

$$\omega_0 = 1.015\sqrt{\frac{E}{\rho}}\frac{w}{L^2} \tag{II.5}$$

$$k_{eff} = 0.658\frac{Ew^3e}{L^3} \tag{II.6}$$

$$m_{eff} = 0.639\rho \cdot Lwe \tag{II.7}$$

E et ρ sont respectivement le module d'Young (en Pa) et la densité (en kg.m^{-3}) du matériau de structure du résonateur.

I.1.3 – Détection

La partie détection a pour but de convertir le déplacement mécanique y de la poutre en un signal électrique à travers un changement de la capacité formée par le système poutre-électrode (Figure II.1.1). En supposant les déplacements faibles par rapport au gap g, le gain de détection κ correspondant à la variation de la capacité δC divisée par le déplacement mécanique y peut être calculé :

$$\kappa = \frac{\delta C(\omega)}{y(\omega)} \approx \frac{\varepsilon_0 ea}{g^2} \text{ [F.m}^{-1}\text{]} \tag{II.8}$$

I.1.4 – Transmission du signal entre le résonateur NEMS et les appareils externes

Pour compléter la fonction de transfert du résonateur NEMS, la transmission de signal entre l'électrode de détection et l'impédance de sortie Z_{out} doit être étudiée. Comme indiqué sur la Figure II.1.4, cette impédance est symbolisée par une capacité C_{out} représentant les capacités de connexion et d'impédance d'entrée de l'appareil de mesure externe.

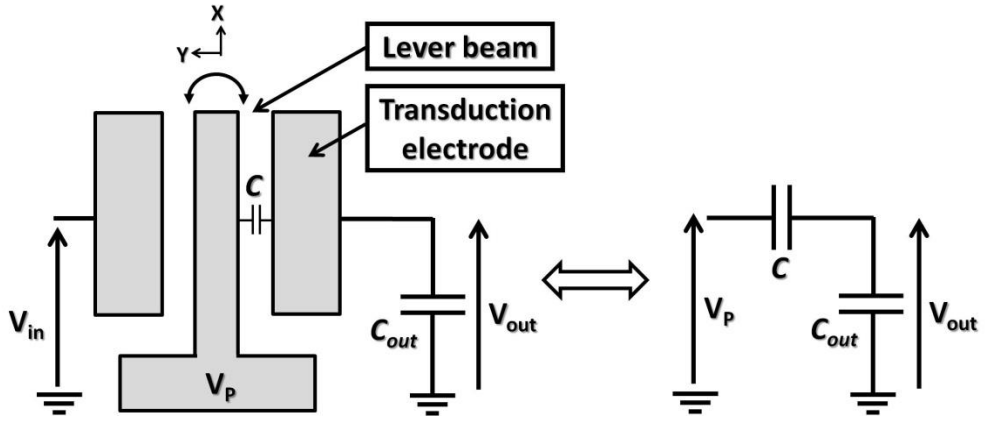


Figure II.1.4: Illustration et schéma électrique équivalent du résonateur NEMS à détection capacitive connecté à une capacité de sortie.

Grâce à ce schéma électrique équivalent, la fonction de transfert R peut être calculée :

$$R = \frac{v_{out}}{\delta C} \approx \frac{V_P - V_{out-dc}}{C + C_{out}} \ [\mathrm{V.F^{-1}}] \qquad \text{(II.9)}$$

II.1.5 – Réponse globale du système

La fonction de transfert totale du résonateur NEMS notée H_{NEMS} correspond au produit de chaque fonction de transfert calculée précédemment :

$$H_{NEMS}(\omega) = \frac{V_{out}}{V_{in}}(\omega) = \frac{V_{out}}{\delta C}(\omega) \cdot \frac{\delta C}{y}(\omega) \cdot \frac{y}{F}(\omega) \cdot \frac{F}{V_{in}}(\omega) = R \cdot \kappa \cdot \alpha(\omega) \cdot J \qquad \text{(II.10)}$$

En conséquence:
$$H_{NEMS}(\omega) = \frac{G_{NEMS}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \qquad \text{(II.11)}$$

avec $$G_{NEMS} \approx \frac{\varepsilon_0^2 e^2 a^2 V_{dc}\left(V_{dc} - V_{out-dc}\right)}{g^4 k_{eff}\left(C + C_{out}\right)} \quad \text{(II.12)}$$

I.2 Modèle électrique équivalent

Une autre approche consiste à modéliser le résonateur NEMS à l'aide de composants électriques. Deux représentations peuvent être utilisées pour analyser les caractéristiques du composant électromécanique à travers sa fonction de transfert $H_{res}(\omega)$.

Le diagramme de Bode consiste à étudier l'évolution du gain $G(\omega)$ (ou $G_{dB}(\omega)$ en dB) et du déphasage $\varphi(\omega)$ en fonction de la pulsation ω.

$$G_{res}(\omega) = |H_{res}(\omega)| \qquad G_{res-dB}(\omega) = 20 \cdot \log_{10}\left[|H_{res}(\omega)|\right] \text{ [dB]} \quad \text{(II.13)}$$

$$\varphi_{res}(\omega) = \arg\left(H_{res}(\omega)\right) \text{ [rad]} \quad \text{(II.14)}$$

Le diagramme de Nyquist représente quant à lui la partie imaginaire de la fonction de transfert $Y(\omega)$ (appelée signal quadratique) par rapport à la partie réelle $X(\omega)$ (appelée composante en phase).

$$X_{res}(\omega) = real\left(H_{res}(\omega)\right) \quad \text{(II.15)}$$

$$Y_{res}(\omega) = imag\left(H_{res}(\omega)\right) \quad \text{(II.16)}$$

Ces deux représentations sont liées par l'équation (II.17).

$$X_{res}(\omega) = G_{res}(\omega) \cdot \cos\left(\varphi_{res}(\omega)\right) \qquad Y_{res}(\omega) = G_{res}(\omega) \cdot \sin\left(\varphi_{res}(\omega)\right) \quad \text{(II.17)}$$

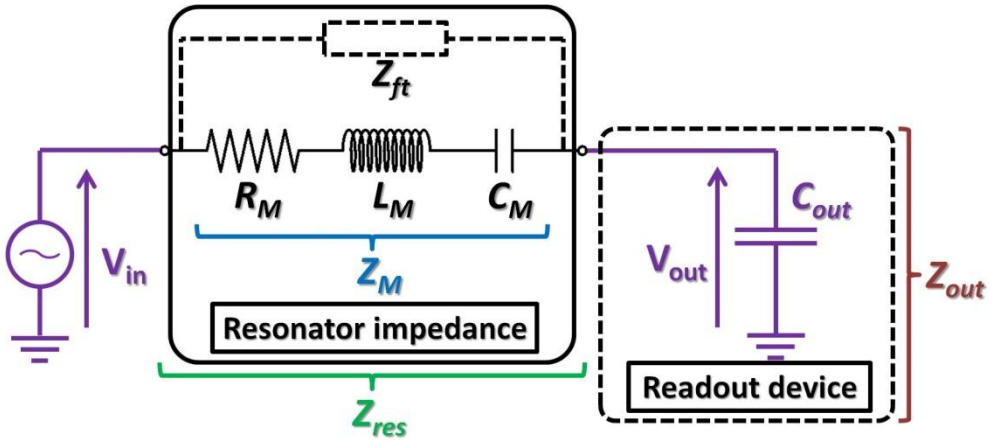


Figure II.1.5: Schéma électrique d'un résonateur NEMS en configuration boucle-ouverte.

Un circuit RLC est généralement utilisé pour modéliser le résonateur. Comme montré sur la Figure II.1.5, deux composantes peuvent être identifiées :

- une partie dite motionnelle $H_{NEMS}(\omega)$ correspondant au signal utile provenant du mouvement de la poutre ;
- une partie dite de fuite $H_{ft}(\omega)$ correspondant à un signal parasite et provenant du passage du signal depuis l'électrode d'actionnement directement vers l'électrode de détection.

La fonction de transfert globale du système est donnée ci-dessous :

$$H_{res}(\omega) \approx \underbrace{\frac{\frac{C_M}{C_{out}}}{1 - L_M C_M \omega^2 + jR_M C_M \omega}}_{H_{NEMS}(\omega)} + \underbrace{\frac{1}{jC_{out} Z_{ft} \omega}}_{H_{ft}(\omega)} \tag{II.18}$$

Par simplification, $H_{NEMS}(\omega)$ peut être réécrite de la manière suivante :

$$H_{NEMS}(\omega) = \frac{G_{NEMS}}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{\omega_0 Q}} \tag{II.19}$$

$$\omega_0 = \sqrt{\frac{1}{L_M C_M}} \tag{II.20}$$

$$Q = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} \tag{II.21}$$

$$G_{NEMS} = \frac{C_M}{C_{out}} \tag{II.22}$$

I.3 Etude théorique

Grâce aux représentations de Bode et de Nyquist, il est possible de déterminer les paramètres caractérisant le résonateur (voir Figure II.1.6)

- La fréquence de résonance f_{res} (ou pulsation ω_{res}) correspond à la fréquence pour laquelle le gain G_{res} et la sensibilité en phase S atteignent leur valeur maximale. En considérant un faible signal de fuite, f_{res} correspond à la fréquence de résonance mécanique de la structure f_0.

- Le facteur de qualité Q est défini comme étant le rapport entre la fréquence de résonance f_{res} et la bande passante Δf à -3dB (II.23).

$$Q = \frac{f_{res}}{\Delta f} = \frac{\omega_{res}}{\Delta \omega} \tag{II.23}$$

- La sensibilité en phase S quant à elle est déterminée par la dérivée du déphasage par rapport à la fréquence. Elle atteint sa valeur maximale à la fréquence de résonance.

$$S(f) = \frac{\partial \varphi}{\partial f} [\text{rad.Hz}^{-1}] \tag{II.24}$$

- Le rapport signal sur fond SBR correspond au rapport du signal total V_{res} (c'est à dire signal motionnel et signal de fond) sur le signal de fond V_{ft} comme défini en (II.25). Il peut également être donné par le rapport du gain du résonateur G_{res} sur le gain de fuite G_{ft}. En pratique, ce ratio est calculé à la fréquence de résonance.

$$SBR(\omega) = \frac{V_{res}(\omega)}{V_{ft}(\omega)} = \frac{G_{res}(\omega)}{G_{ft}(\omega)} \tag{II.25}$$

En modélisant l'impédance Z_{ft} de fond comme une capacité parasite C_{ft}, la fonction de transfert H_{ft} est constante et ne dépend plus de la fréquence. Cette valeur de fond a une forte influence sur les performances du résonateur, comme illustré sur la Figure II.1.6.

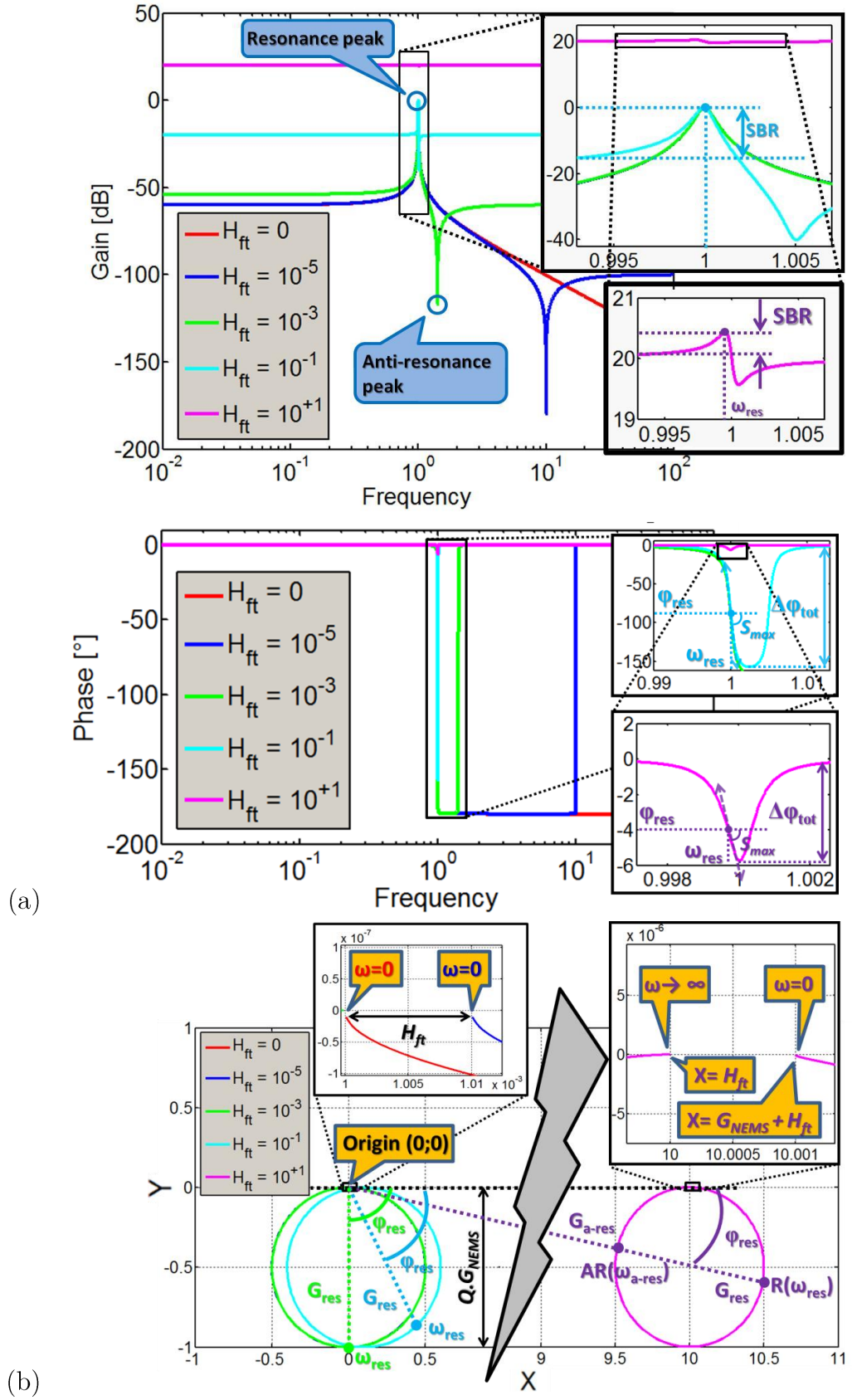


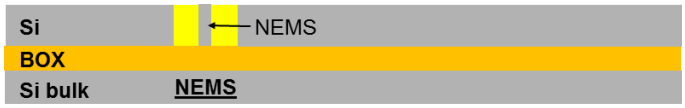
Figure II.1.6: Diagramme de Bode (a) et de Nyquist (b) d'un résonateur avec différents niveaux de fond. Les encarts en (a) et (b) correspondent à des zooms près de la fréquence de résonance. G_{NEMS} et Q sont fixés respectivement à 10^{-3} et 10^{3}.

II. Etude d'un démonstrateur NEMS-CMOS co-intégré en 2D

II.1 Procédé de fabrication

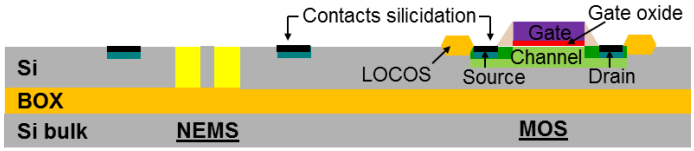
Le procédé de fabrication est exposé en Figure II.2.1. La fabrication suit une stratégie d'élaboration pré-CMOS dans laquelle le NEMS est réalisé avant le circuit électronique.

1



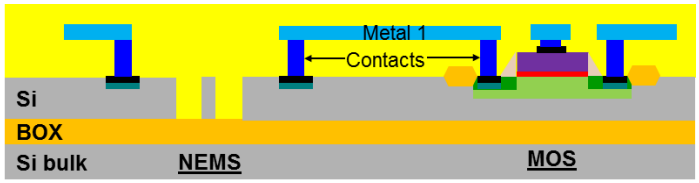
Litho-gravure des NEMS, remplissage des espaces et aplanissement.

2



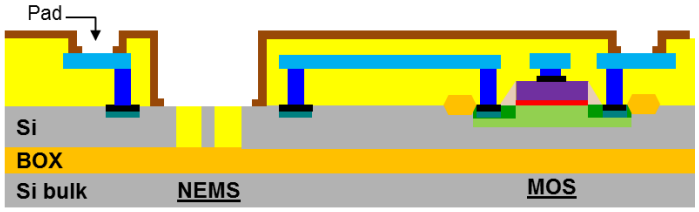
Procédé front-end CMOS, dopage et siliciuration des contacts MOS et NEMS.

3



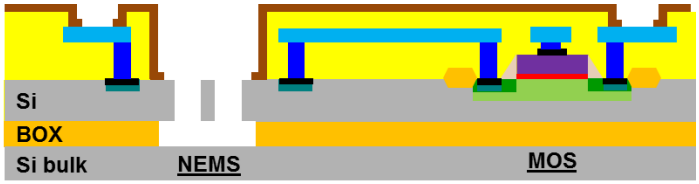
Procédé back-end CMOS.

4



Ouverture du back-end suivi d'une étape de dépôt et de litho-gravure d'une couche protectrice (HfO_2 ici).

5



Libération des NEMS à l'HF(acide fluorhydrique) vapeur.

Figure II.2.1: Procédé de fabrication du système NEMS-CMOS étudié [Arc12].

II.2 Design du démonstrateur

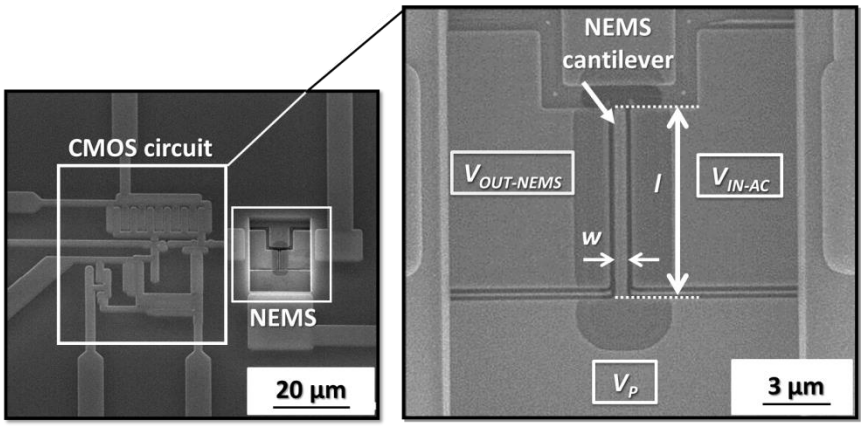


Figure II.2.2: Image MEB du dispositif NEMS-CMOS (à gauche) et zoom sur le résonateur NEMS (à droite) (l=8.3µm, w=0.5µm, g=0.25µm). l, w, g correspondent respectivement à la longueur, la largeur de la poutre et à l'espace entre les électrodes et le cantilever.

La Figure II.2.2 montre une vue MEB du dispositif NEMS-CMOS et du résonateur NEMS. Ce dernier comprend une poutre encastrée-libre avec un actionnement électrostatique et une détection capacitive. Six designs différents ont été proposés dont les caractéristiques sont décrites en Tableau II.1. Le module d'Young E et la densité ρ sont respectivement de 160GPa et de 2330kg.m^{-3}, correspondant à des valeurs typiques pour le c-Si.

Le circuit CMOS quant à lui fournit un gain et un déphasage adéquat pour permettre de satisfaire les conditions de Barkhausen pour le système NEMS-CMOS. Ce circuit électronique est monolithiquement lié à la partie mécanique, permettant ainsi de limiter drastiquement les pertes par atténuation du signal. Un design simple est proposé : sept transistors répartis en deux blocs différents : un étage d'amplification fournissant le gain et le déphasage suffisant et un étage de buffer unitaire permettant l'adaptation d'impédance avec les appareils externes. Le schéma électrique global du circuit est présenté en Figure II.2.3. Les dimensions des transistors sont détaillées en Tableau II.2. Deux types de dispositifs ont été fabriqués pour chaque design de NEMS : une boucle ouverte et une boucle fermée, dont la sortie de l'amplificateur CMOS est directement reliée à l'entrée du NEMS (contrairement à la boucle ouverte).

Dispositifs	PEL1P	PEL2P	PEL3P	PEL4P	PEL5P	PEL6P
l (µm)	5.9	8.3	8.3	11.7	4.1	5.9
w (µm)	0.25	0.5	0.25	0.5	0.25	0.5
f_0 (MHz)	9.88	9.99	4.99	5.03	20.5	19.8

Tableau II.1: Dimensions des résonateurs et valeurs des fréquences de résonance pour chaque design.

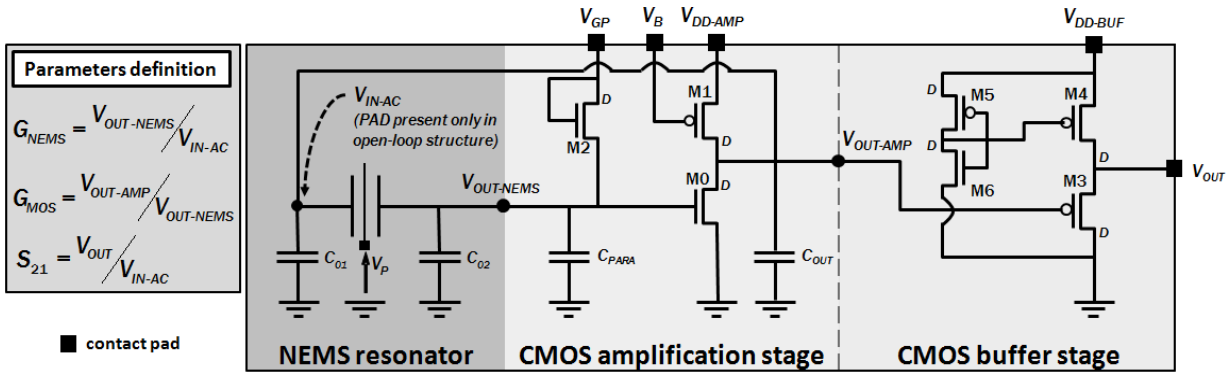


Figure II.2.3: Schéma électrique de l'auto-oscillateur NEMS-CMOS et définition des paramètres principaux de la cellule oscillante (sur la gauche). D indique l'emplacement des drains pour chaque transistor.

Transistors	M0	M1	M2	M3,6	M4	M5
W (µm)	1.2	6.7 (x10)	1	10	4	0.8
L (µm)	0.5	1	1	0.5	0.625	0.5

Tableau II.2: Dimensions de chaque transistor CMOS transistor.

II.3 Comparaison

Le Tableau II.3 présente une comparaison entre le dispositif étudié dans cette thèse et d'autres systèmes NEMS-CMOS décrits dans la littérature.

Deux architectures différentes peuvent être utilisées dans la constitution de cellules oscillantes à base de NEMS-CMOS : les PLL (ou boucles à verrouillage de phase) et les boucles auto-oscillantes. Le dispositif décrit dans cette thèse utilise cette dernière approche, ce qui lui permet d'être le dispositif le plus compact jamais conçu jusqu'à ce jour (les dimensions mentionnées dans le tableau ne comprennent pas les plots métalliques).

Références	**Technologie utilisée**	**Matériau et forme du résonateur**	**Fréquence de résonance (MHz)**	**Aire du pixel(µm²)**
[Nab09]	0.18µm	SiC / poutre	8.29 and 11.59	6250000
[Li12]	TSMC 0.35µm	Métal / peigne interdigité	0.117	298000
[Zal10]	ON S. 1.5µm	Si poly / dôme	10-100	63000
[Ver08]	AMS 0.35µm	Métal / poutre	6.32	60000
[Pac13]	TSMC 0.35µm	Métal / anneau	1.39 and 9.34	37700
[Hua08]	TSMC 0.35µm	Nickel / disque	10.92	20600
Ce travail	ST 0.35µm	Si mono / poutre	7-8	3500

Tableau II.3: Comparaison de différents oscillateurs co-intégrés NEMS-CMOS présents dans la littérature. ON S signifie ON Semiconductor.

II.4 Caractérisation du dispositif NEMS-CMOS

La meilleure solution pour fabriquer un détecteur de masse à base de résonateurs NEMS le plus dense possible est d'utiliser une architecture de boucle oscillante. Les valeurs des tensions électriques appliquées au système pour satisfaire les conditions de Barkhausen doivent être déterminées. Une première étape de caractérisation des dispositifs en boucle ouverte est primordiale.

II.4.1 – Analyse du fonctionnement du circuit CMOS

La Figure II.2.4 représente le schéma électrique équivalent simplifié de l'amplificateur CMOS en petit signal. En choisissant un design judicieux, il est possible de simplifier le fonctionnement de ce circuit et d'obtenir une expression simple de la fonction de transfert du circuit d'amplification CMOS :

$$H_{AMP-MOS} = \frac{V_{OUT-AMP}}{V_{OUT-NEMS}}(\omega_{res}) \approx -\frac{g_{m-M_0}}{jC_{OUT}\omega_{res}} \approx j\frac{g_{m-M_0}}{C_{OUT}\omega_{res}} \quad \text{(II.26)}$$

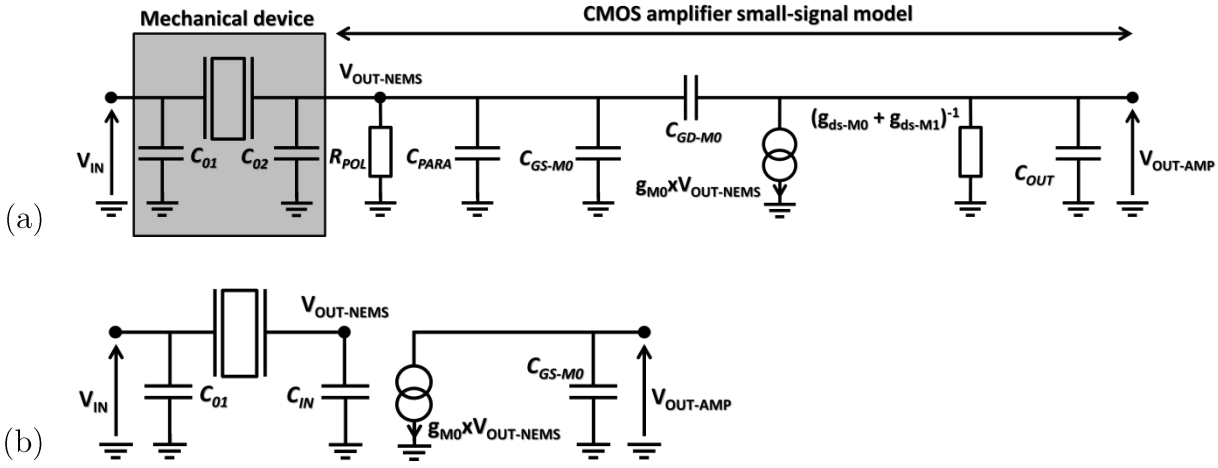


Figure II.2.4: Modèle petit signal du résonateur NEMS et de l'amplificateur CMOS avant (a) et après (b) simplification.

C_{IN} correspond ici à la capacité totale entre le résonateur et le transistor M_0, C_{02}, C_{PARA} et C_{GS-M0} étant respectivement la capacité entre la poutre et l'électrode de détection, la capacité parasite en sortie de NEMS et la capacité de grille-source du transistor M_0 :

$$C_{IN} = C_{02} + C_{PARA} + C_{GS-M_0}\,[\mathrm{F}] \quad \text{(II.27)}$$

Par conséquent, le gain et le déphasage de l'amplificateur CMOS deviennent à la résonance:

$$G_{AMP-MOS}(\omega_{res}) = \frac{g_{m-M_0}}{C_{OUT}\omega_{res}} \qquad \text{and} \qquad \varphi_{AMP-MOS}(\omega_{res}) = 90° \qquad \text{(II.28)}$$

II.4.2 – Caractérisation en boucle ouverte

Dans le cadre de cette thèse, les caractérisations électriques furent réalisées dans une chambre à vide (voir Figure II.2.5) avec un analyseur de réseau calibré selon le câblage utilisé. La pression à l'intérieur de la chambre fut fixée à 0,05mbar.

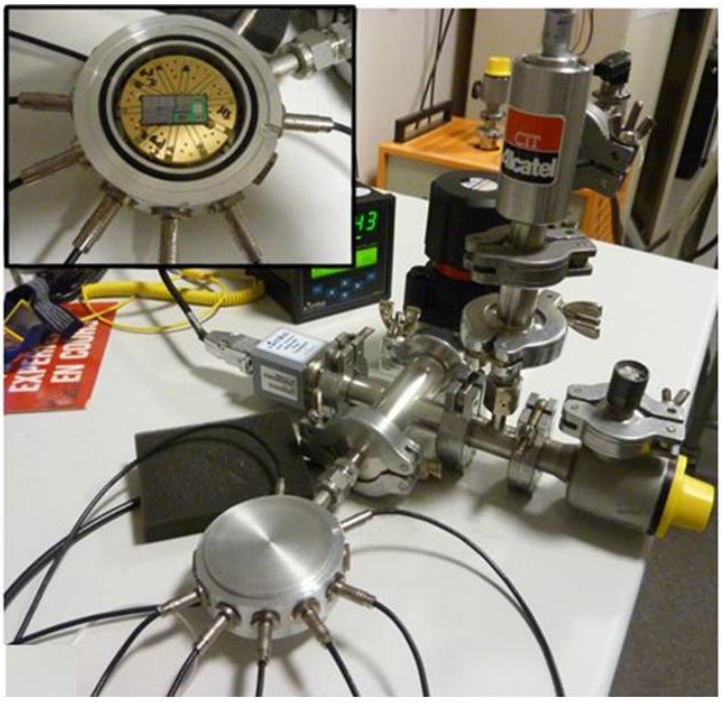


Figure II.2.5: Chambre à vide utilisée pour caractériser les dispositifs placés sur un PCB, le tout disposé dans la chambre à vide.

III.4.2.1: Caractérisation de la cellule NEMS-CMOS

Afin de démontrer l'intérêt électrique d'une co-intégration NEMS-CMOS, la réponse fréquentielle de deux résonateurs de même dimension est comparée. L'un correspond à un dispositif monolithiquement intégré avec un circuit CMOS, l'autre se trouve en configuration dite « stand-alone » (c'est-à-dire sans de circuit juxtaposé), ces deux résonateurs étant sur la même puce. La Figure II.2.6 montre une amélioration nette de 63dB du signal pour le système co-intégré à la résonance (évaluée à 8.6MHz). Cette amélioration est en particulier due à la différence de capacités parasites C_{PARA} nettement plus importante dans le cas « stand-alone » que dans le cas co-intégré.

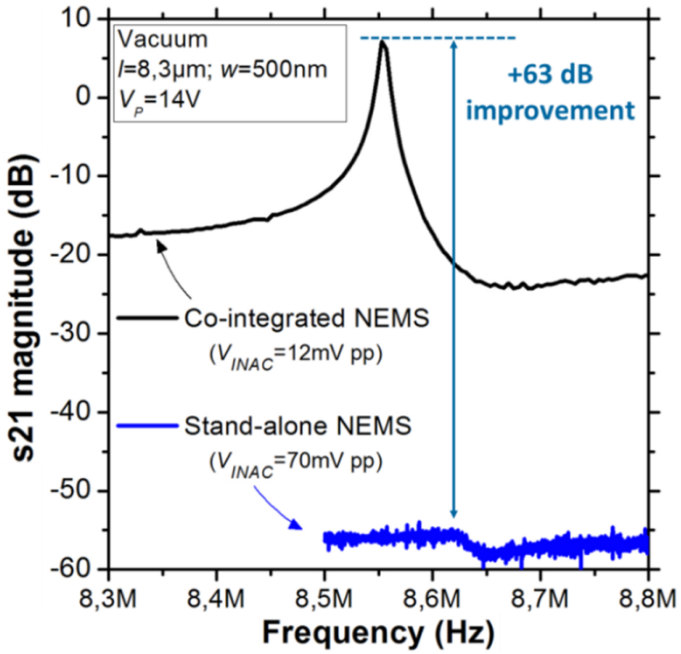
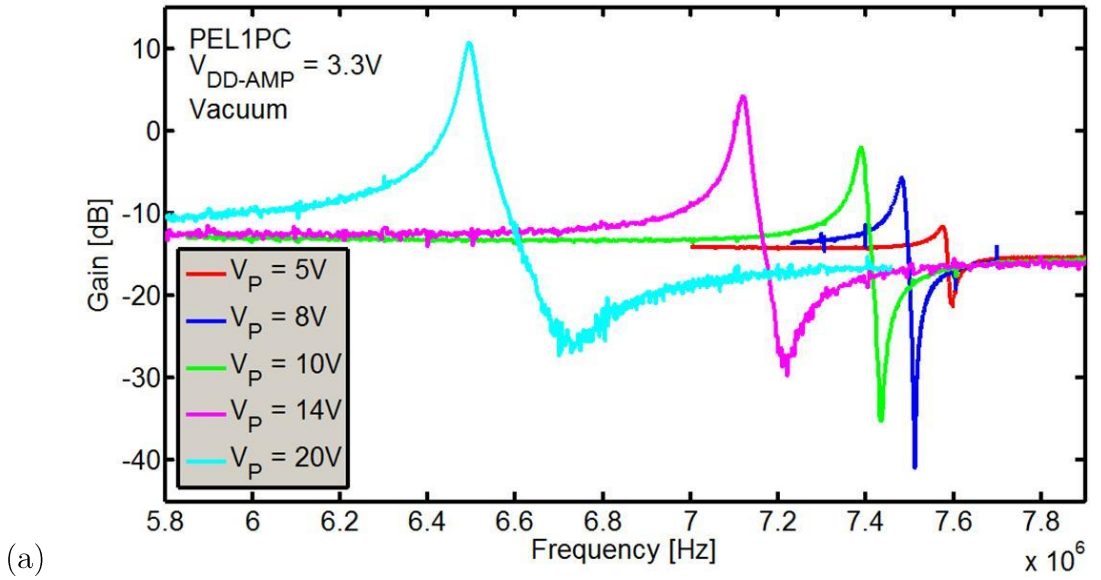
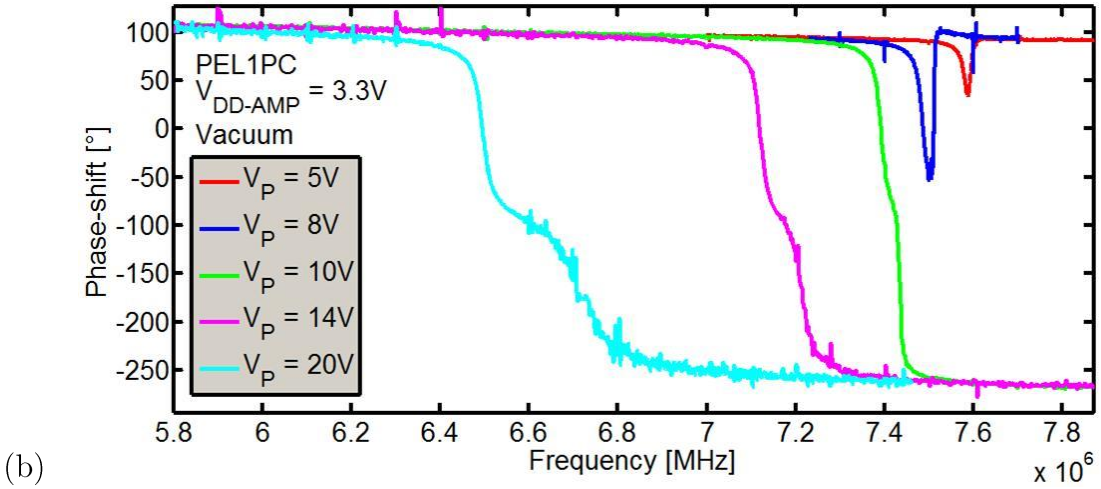


Figure II.2.6: Comparaison des réponses fréquentielles d'un résonateur en configuration « stand-alone » et co-intégré avec un circuit CMOS (s21 est défini en Figure II.2.3). Une tension d'alimentation $V_{DD\text{-}AMP}$ de 2V est appliquée dans le cas du système co-intégré [Arc12].

La réponse fréquentielle de différents dispositifs NEMS fut étudiée pour une même tension d'entrée V_{IN} et pour différentes tensions de cantilever V_P. Les courbes expérimentales sont exposées en Figure II.2.7. Comparé au cas théorique, un déphasage plus important est observé pour des hautes valeurs de V_P et peut être expliqué par les effets combinés du signal de fuite et du déphasage du circuit CMOS.



(a)



(b)

Figure II.2.7: Diagramme de Bode en gain (a) et en déphasage (b) d'un système NEMS-CMOS utilisant une structure PEL1P.

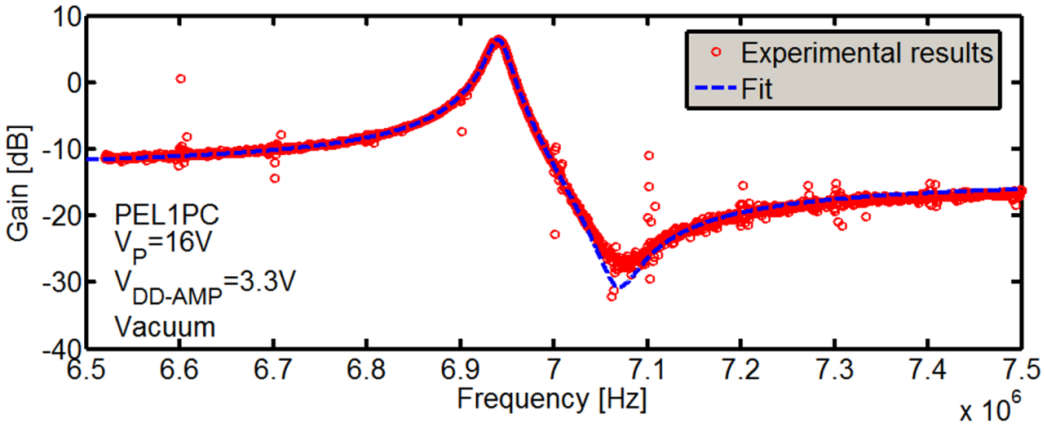
III.4.2.2: Extraction et analyse des paramètres

Ces réponses fréquentielles ont été ensuite modélisées en utilisant les expressions (II.29) et (II.30) afin d'extraire les paramètres du résonateur : f_{res}, Q, and G_{NEMS} pour chaque V_P. Pour la modélisation, la fonction de transfert de fuite est exprimée par un nombre complexe avec $H_{ft\text{-}real}$ et $H_{ft\text{-}imag}$ respectivement en tant que parties réel et imaginaire. De plus, un déphasage ψ supplémentaire provenant du circuit CMOS est pris en compte. V_{dc} et $V_{out\text{-}dc}$ correspondent respectivement aux tensions V_P et V_{GP}.

$$H_{res}(f)=\left(\frac{G_{NEMS}}{1-\left(\frac{f}{f_{res}}\right)^2+j\frac{f}{f_{res}Q}}+H_{ft-real}+jH_{ft-imag}\right)G_{MOS}e^{j\Psi} \qquad \text{(II.29)}$$

avec
$$G_{NEMS}=\frac{\varepsilon_0^2 e^2 a^2 V_{dc}\left(V_{dc}-V_{out-dc}\right)}{g^4 k C_{IN}} \qquad \text{(II.30)}$$

(a)



(b)

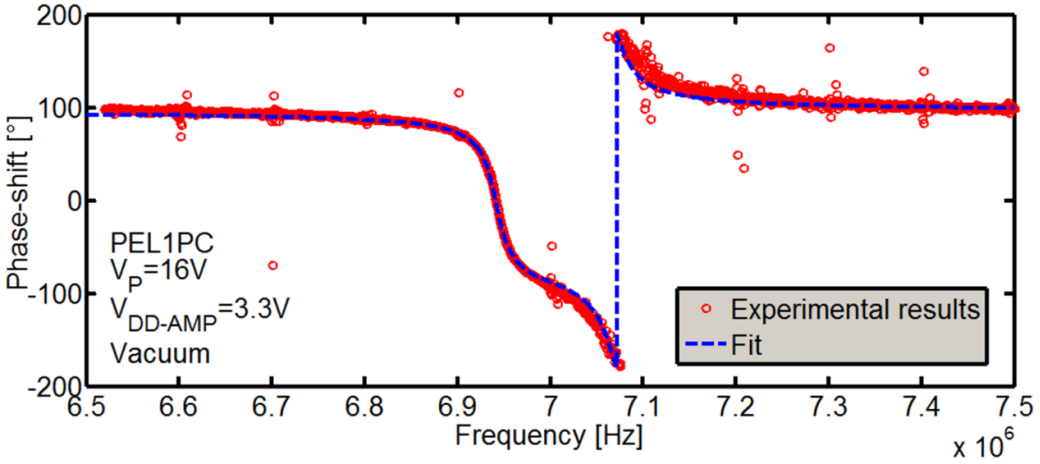


Figure II.2.8: Résultats expérimentaux et modélisation du diagramme de Bode pour V_P=16V.

Comme observé dans la Figure II.2.7, la fréquence de résonance f_{res} semble diminuer lorsque V_P augmente, ceci en raison de l'effet dit de « spring softening effect ». Les forces électrostatiques générées à cause des tensions d'actionnement $V_{in\text{-}AC}$, de détection V_{GP} et de poutre V_P tendent à écranter l'effet de la force de rappel. Ceci a pour conséquence de diminuer virtuellement la constante de raideur du résonateur (II.31) lorsque la tension V_P augmente.

$$m\ddot{y} + c\dot{y} + \underbrace{\left(k_0 - \frac{\varepsilon_0 ea}{g^3}\left[V_P^2 + (V_P - V_{GP})^2\right]\right)}_{k} y \approx \underbrace{\frac{\varepsilon_0 ea}{2g^2}\left[V_{GP}(2V_P - V_{GP})\right]}_{F_{elec}} \qquad \text{(II.31)}$$

Grâce aux relations (II.12) et (II.31) et grâce aux courbes de modélisation de f_{res}, Q et G_{NEMS} (voir Figures II.2.9, II.2.10 et II.2.11), la détermination des capacités parasites parasites a pu être possible à la fois pour le cas « stand-alone » et le cas co-intégré (voir Figure II.2.12).

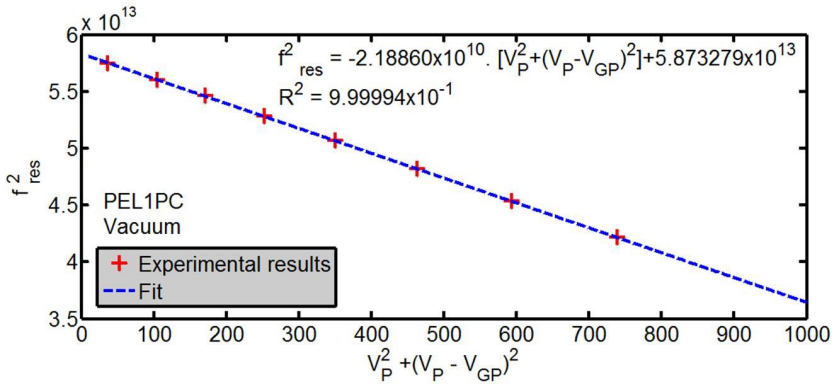


Figure II.2.9: Evolution de la fréquence de résonance en fonction des tensions de polarisation de la poutre V_P et de la grille du transistor M_0 V_{GP}. R^2 correspond au coefficient d'autocorrélation entre la modélisation et les résultats expérimentaux.

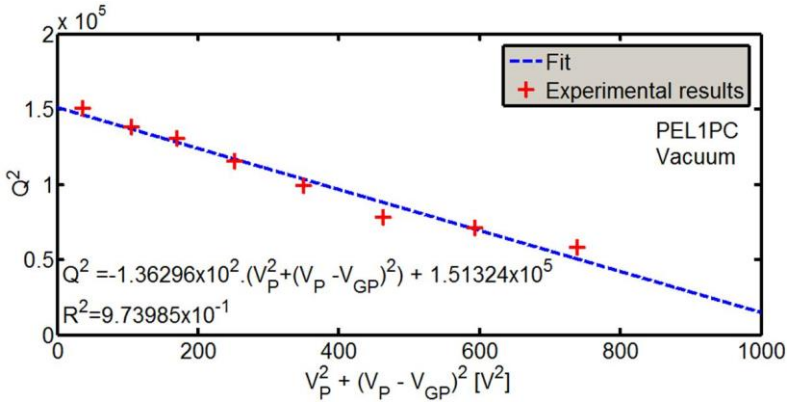


Figure II.2.10: Variation du facteur de qualité en fonction des tensions de polarisation de la poutre et de la grille du transistor M_0.

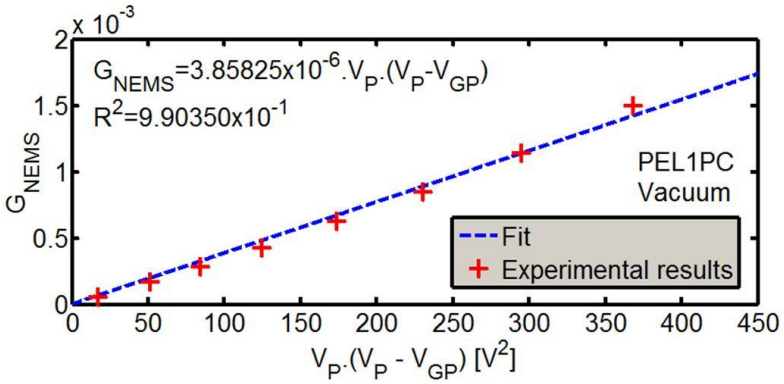


Figure II.2.11: Variation du gain du NEMS à la résonance G_{NEMS} en fonction des tensions de polarisation de la poutre et de la grille du transistor M_0.

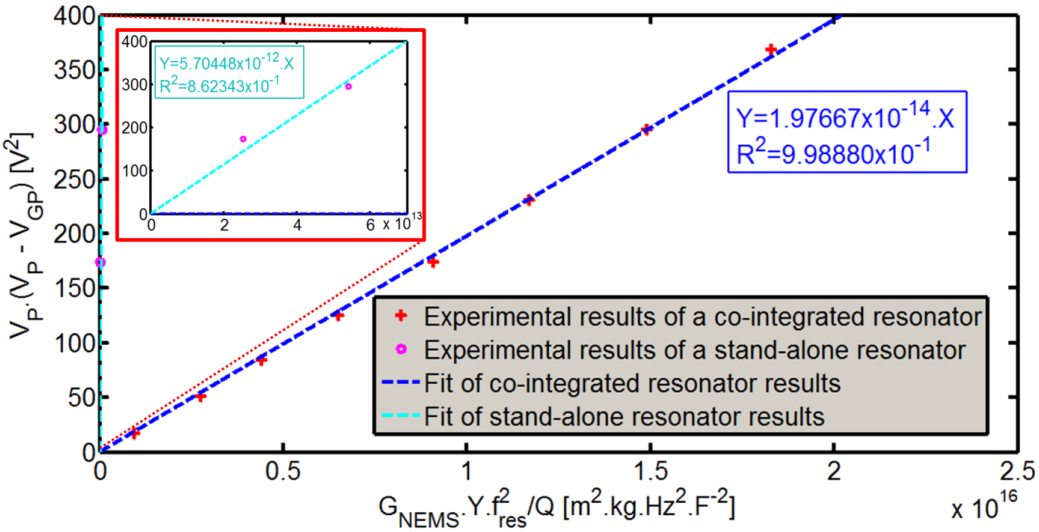


Figure II.2.12: Détermination des capacités parasites C_{PARA} pour une configuration « stand-alone » (en bleu ciel) et co-intégrée (en bleu foncé).

Les valeurs des capacités parasites sont données par le coefficient directeur des pentes en Figure II.2.12. Ces capacités valent 19.8fF et 5.70pF respectivement pour le cas « stand-alone » et le cas co-intégré, validant l'intérêt électrique de l'intégration monolithique.

II.4.3 – Caractérisation en boucle fermée et réalisation d'une boucle auto-oscillante.

Afin de réaliser une boucle auto-oscillante, la fonction de transfert de la cellule NEMS-CMOS en boucle ouverte $H_{OL}(f)$ doit respecter des conditions particulières appelées conditions de Barkhausen.

$H_{OL}(f)$ est défini comme le produit des fonctions de transfert du résonateur $H_{res}(f)$ et du circuit électronique de rebouclage $H_{elec}(f)$.

$$H_{OL}(f) = H_{elec}(f) \cdot H_{res}(f) \tag{II.32}$$

Les auto-oscillations apparaissent à une fréquence f_{osc} si et seulement si deux critères sont respectés, à savoir :

$$\left|H_{OL}(f_{osc})\right| \geq 1 \qquad \text{et} \qquad \arg\left[H_{OL}(f_{osc})\right] = 0° \tag{II.33}$$

(II.33) étant équivalent à:

$$\begin{cases} G_{res}(f_{osc}) \cdot G_{elec}(f_{osc}) \geq 1 \\ \varphi_{res}(f_{osc}) + \varphi_{elec}(f_{osc}) = 0° \end{cases} \tag{II.34}$$

En conséquence, le circuit électronique (en particulier l'étage d'amplification) doit être judicieusement conçu et alimenté de telle manière à mettre le système en oscillation. La conception du circuit dépend directement des paramètres et des caractéristiques du résonateur NEMS.

D'autre part, les amplitudes d'oscillation du résonateur doivent être contrôlées. Par souci de sécurité, cette amplitude est limitée à seulement 50% de la distance g. Cette limitation est assurée par la saturation du circuit d'amplification. Cette méthode permet d'avoir un circuit simple et très compact. Or, cette limitation est d'autant plus grande que la tension d'alimentation $V_{DD\text{-}AMP}$ est faible. Afin de garantir l'intégrité du dispositif, il est donc nécessaire d'opérer à des tensions d'alimentation du circuit amplificateur faible.

En prenant en compte toutes ces considérations, la mise en auto-oscillation de la cellule NEMS-CMOS fut possible. Les Figures II.2.13 et II.2.14 montrent (respectivement dans le domaine temporel et fréquentiel) la réalisation d'un auto-oscillateur générant un signal à 7,83MHz avec une amplitude rms de 0,18mV sans la présence d'oscillation parasite sur un large spectre en fréquence. Ce résultat montre le grand intérêt de l'intégration monolithique NEMS-CMOS pour la génération d'oscillateur.

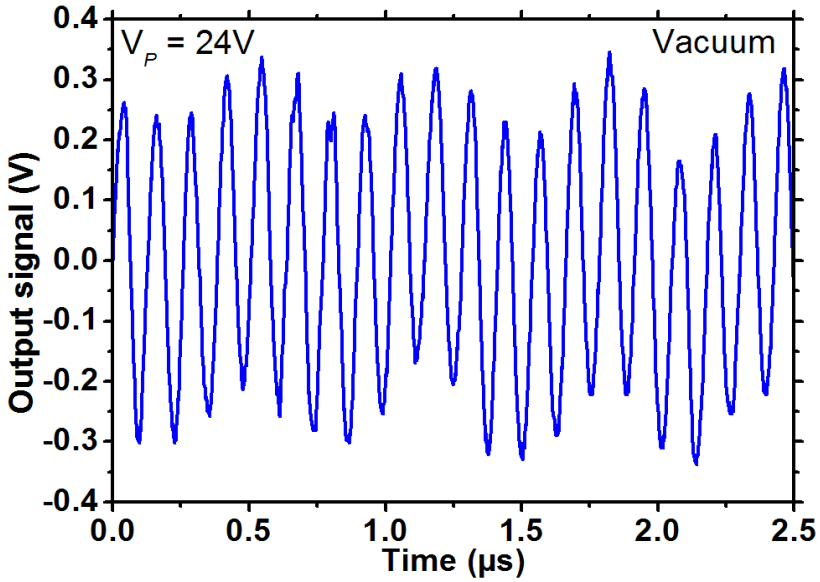


Figure II.2.13: Signal de sortie V_{OUT} dans le domaine temporel de la boucle fermée NEMS-CMOS et obtenue sous vide (0,05mbar).

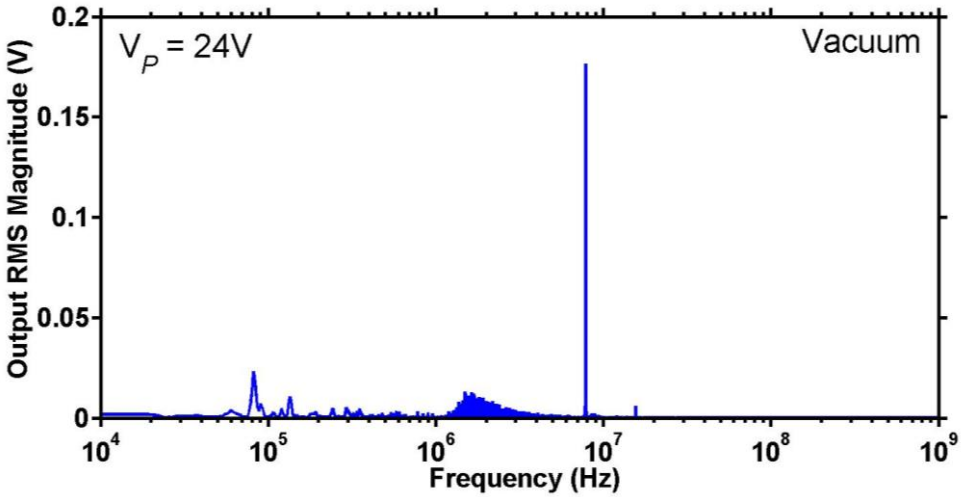


Figure II.2.14: Transformée de Fourrier du signal de sortie V_{OUT}. Le signal de l'oscillateur NEMS-CMOS correspond au plus grand pic.

III. Discussion et conclusion

Ce chapitre a permis de présenter un modèle pour expliquer le fonctionnement et extraire les paramètres principaux d'une cellule NEMS-CMOS, avec un résonateur NEMS à actionnement et détection capacitive réalisé en c-Si. Grâce à cette extraction et à la caractérisation de ce dispositif, les tensions appliquées au niveau du résonateur et du circuit CMOS nécessaires pour satisfaire les conditions de Barkhausen ont pu être déterminées. De ce fait, une boucle auto-oscillante NEMS-CMOS très compacte a pu être réalisée tout en assurant un contrôle des amplitudes d'oscillation de la poutre. Cette architecture constitue un dispositif intéressant pour le développement de réseau d'auto-oscillateurs NEMS-CMOS très compacts en vue des applications de détection de masse.

Le résonateur est fabriqué suivant une intégration 2D à côté du circuit électronique. Cette architecture peut être davantage optimisée afin d'améliorer la densité de NEMS en surface, en construisant ceux-ci au-dessus du circuit et des interconnexions. Le chapitre suivant présente plus en détail le développement d'une telle architecture.

Chapitre III

Développement d'une technologie de co-intégration 3D NEMS-CMOS

Dans le chapitre précédent a été présenté un auto-oscillateur NEMS-CMOS co-intégré en 2D. Ce troisième chapitre se propose d'étudier la démonstration et la faisabilité d'une nouvelle intégration monolithique consistant à implémenter un nano-résonateur en c-Si au-dessus d'un circuit CMOS et de ses interconnexions.

I. Présentation de l'intégration 3D NEMS-CMOS

I.1 Problématique

Le chapitre 1 nous a montré que l'approche hybride pour intégrer NEMS et CMOS avait de forts inconvénients, tels que de fortes capacités parasites provoquant des pertes d'information. Le réseau de résonateurs est également affecté non seulement à cause du pas à respecter entre chaque interconnecteur (comme les TSVs avec la KOZ), mais également en raison de l'imprécision d'alignement lors de la fabrication de larges interconnecteurs (voir Figure III.1.1).

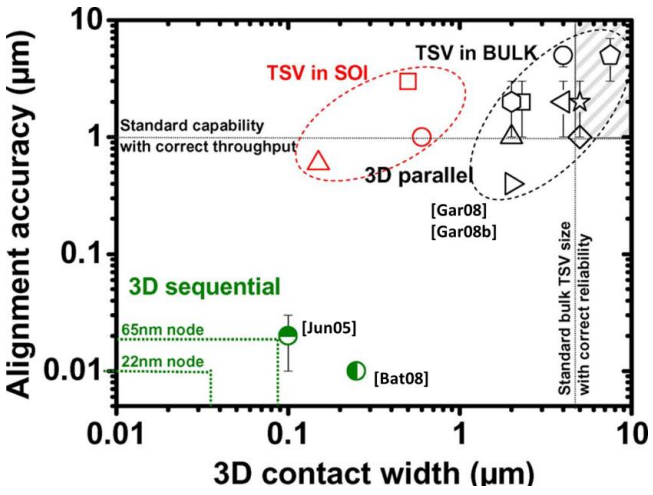


Figure III.1.1: Variation de la précision d'alignement par rapport à la taille du contact pour des approches hybrides (parallèles) et séquentielles (monolithiques) dans le cas d'intégration 3D [Bat12].

Le collage direct métal-oxyde constitue une alternative intéressante puisqu'elle permet de faire intervenir des contacts de petite dimension. L'inconvénient majeur provient des contraintes de topologie et d'alignement des substrats avant l'étape de collage afin de garantir la connectivité électrique.

Afin de réaliser le résonateur mécanique en c-Si, deux options sont possibles. La réalisation FE de la partie mécanique a été étudiée. L'inconvénient majeur de cette intégration est la surface prise par la cellule NEMS-CMOS. Pour contourner cette difficulté, l'intégration ne doit plus se faire en 2D, mais en 3D. Une possibilité consiste à réaliser un collage moléculaire (oxyde-oxyde) entre une plaque CMOS et une plaque SOI à implémenter la partie mécanique au niveau de la zone active de cette dernière.

II. Procédé de fabrication d'un dispositif NEMS-CMOS co-intégré en 3D

II.1 Description du procédé

Dans cette section est décrit le procédé de fabrication afin d'intégrer monolithiquement en 3D une cellule NEMS-CMOS en réalisant le résonateur au-dessus du circuit CMOS et des interconnexions. Cette thèse propose d'évaluer la faisabilité d'une telle technologie. Deux substrats doivent être utilisés pour sa réalisation : un substrat SOI servant à la réalisation des NEMS et un substrat CMOS contenant à la fois circuit et interconnexions. Une préparation de ces deux supports est préalablement nécessaire avant l'assemblage.

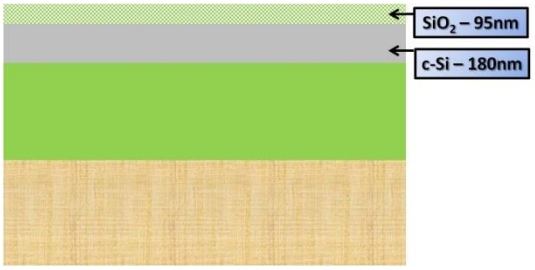
II.1.1 – Préparation des substrats SOI

La Figure III.2.1 décrit le procédé de préparation des substrats SOI. Ces types de substrats permettent de réaliser les résonateurs en c-Si. Les étapes de hautes températures (recuit d'activation et de diffusion des dopants) ont lieu sur ces substrats et avant assemblage afin de ne pas endommager les interconnexions du substrat CMOS.

1

Substrat SOI avec 400nm de BOX et 205nm de c-Si.

2



Oxydation thermique (1050°C) pour amincissement de la couche de c-Si.

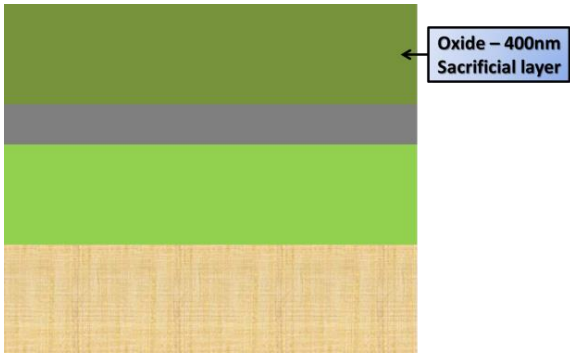
3

Gravure humide du SiO_2 formé par recuit (température ambiante).

4

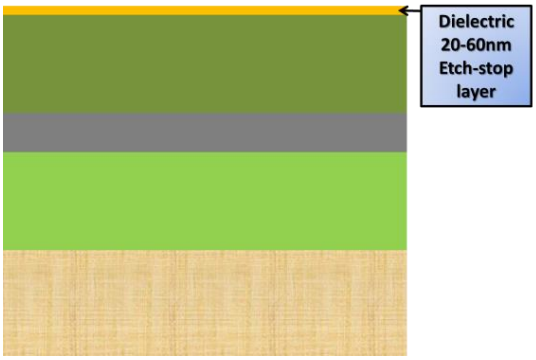
Dopage par implantation de bore et recuit thermique (800°C and 1050°C).

5



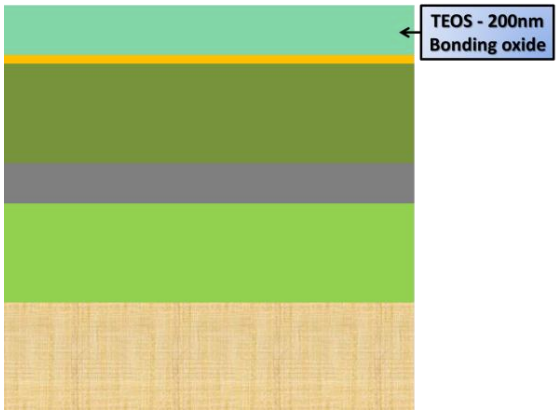
Dépôt d'oxyde pour formation de la couche sacrificielle (400nm) et recuit thermique (750°C).

6



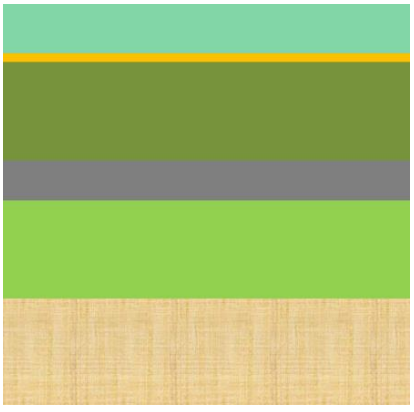
Dépôt d'un diélectrique pour formation d'une couche d'arrêt (20-60nm) et recuit thermique (selon le matériau).

7



Dépôt d'oxyde en tant qu'oxyde de collage (TEOS 200nm déposé à 400°C)

8



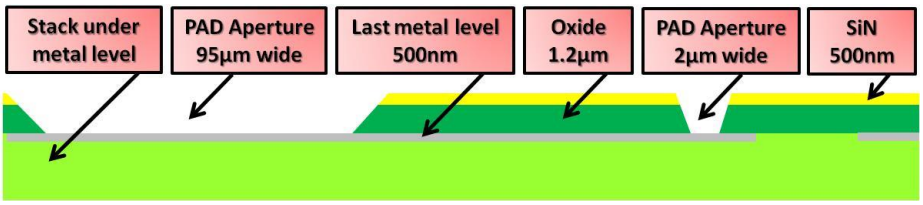
Recuit thermique de l'oxyde de collage pour déshydratation (400°C)

Figure III.2.1: Préparation des substrats SOI.

II.1.2 – Préparation des substrats CMOS

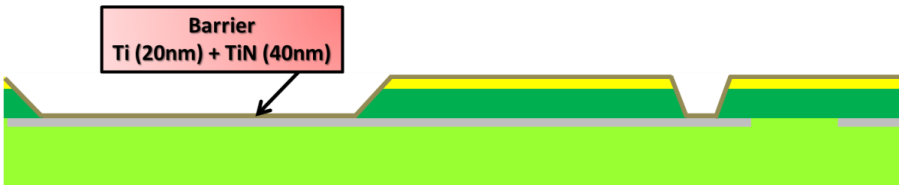
La préparation des substrats CMOS a lieu en parallèle de celle des substrats SOI. Dans le cadre de cette thèse, une technologie AMS 0,35µm utilisant quatre niveaux de métaux d'interconnexion a été sélectionnée. La Figure III.2.2 décrit la préparation des substrats CMOS (ceux-ci sont dessinés avec seulement le dernier niveau de métal pour simplification).

1



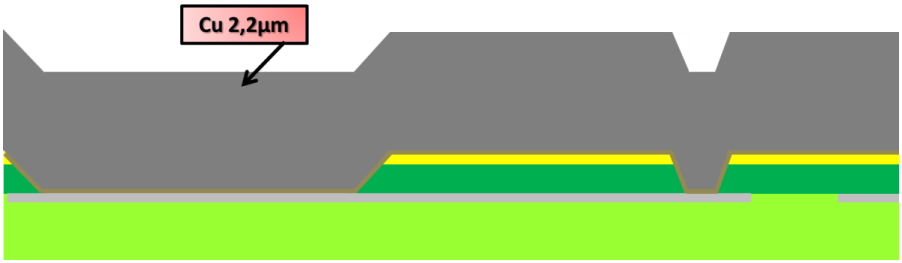
Description des substrats CMOS. Ceux-ci présentent des accès au dernier niveau de métal.

2



Dépôt PVD et CVD d'une barrière Ti-TiN (380°C maximum).

3

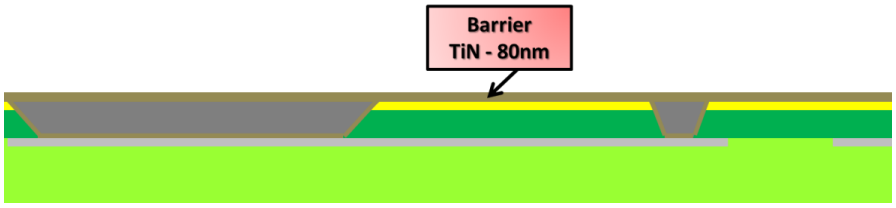


Dépôt PVD, CVD et ECD de Cu (température ambiante) et recuit thermique (250°C maximum).

4

Aplanissement du Cu et du TiN (température ambiante).

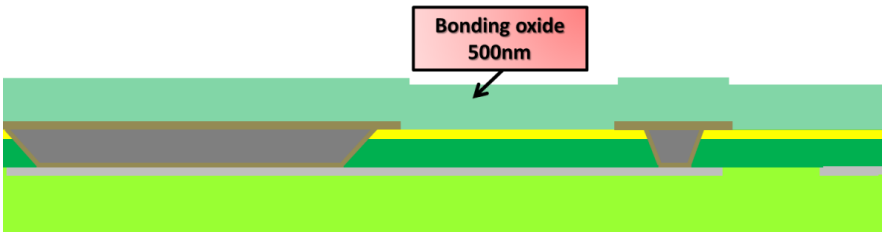
5



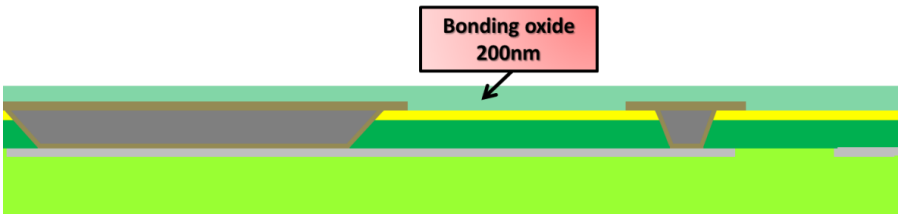
Dépôt CVD et PVD d'une barrière TiN (380°C maximum).

6 

Lithographie UV (DUV) et gravure de la barrière TiN (température ambiante).

7 

Dépôt d'oxyde pour le collage (TEOS déposé à 400°C).

8 

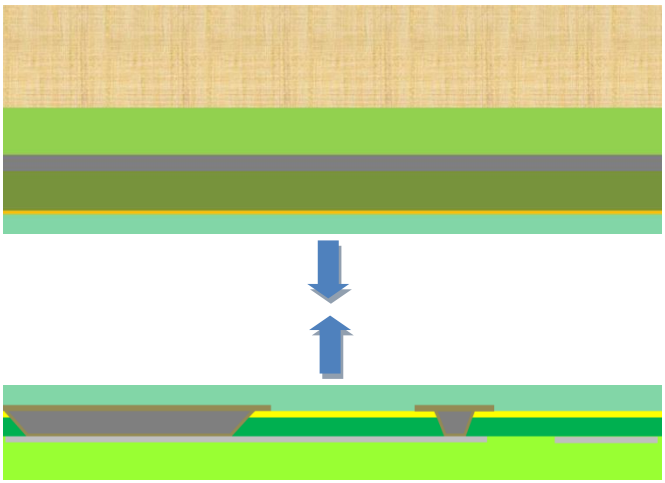
Aplanissement de l'oxyde et recuit thermique pour déshydratation (400°C).

Figure III.2.2: Préparation des substrats CMOS.

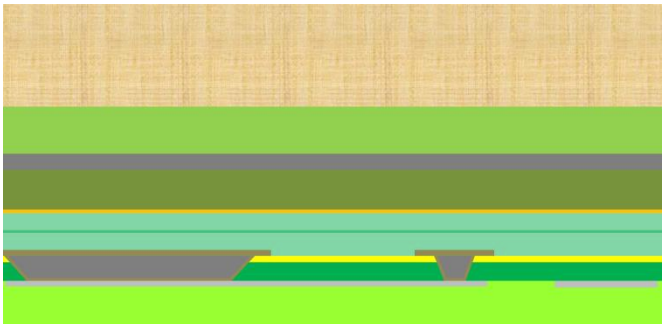
II.2.3 – Assemblage final

Après la préparation des deux substrats, leur assemblage par collage moléculaire peut avoir lieu. Le procédé d'assemblage est présenté en Figure III.2.3.

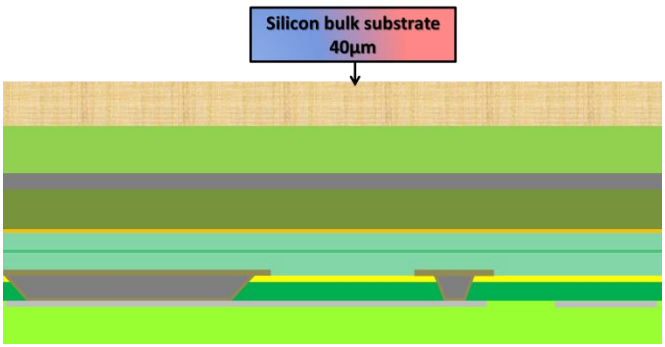
L'assemblage étant opéré, la réalisation des NEMS et des interconnexions entre résonateurs et niveaux métalliques peut avoir lieu. Les températures lors de tout le procédé (présenté en Figure III.2.4) ne doivent pas dépasser les 450°C afin de ne pas endommager les éléments du substrat CMOS.



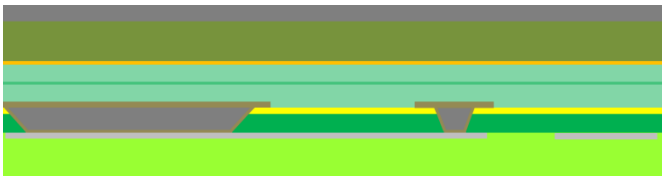
1 Léger aplanissement des deux oxydes de surface et préparation du collage (température ambiante).



2 Collage moléculaire et recuit thermique (400°C).

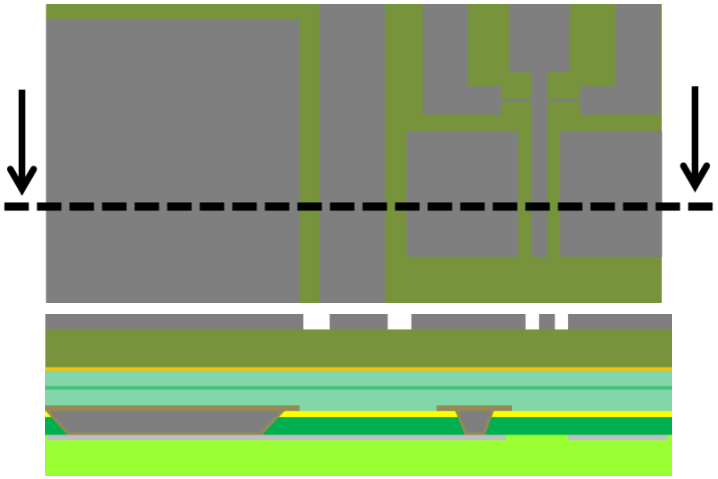


3 Amincissement mécano-chimique du silicium bulk du substrat (température ambiante).

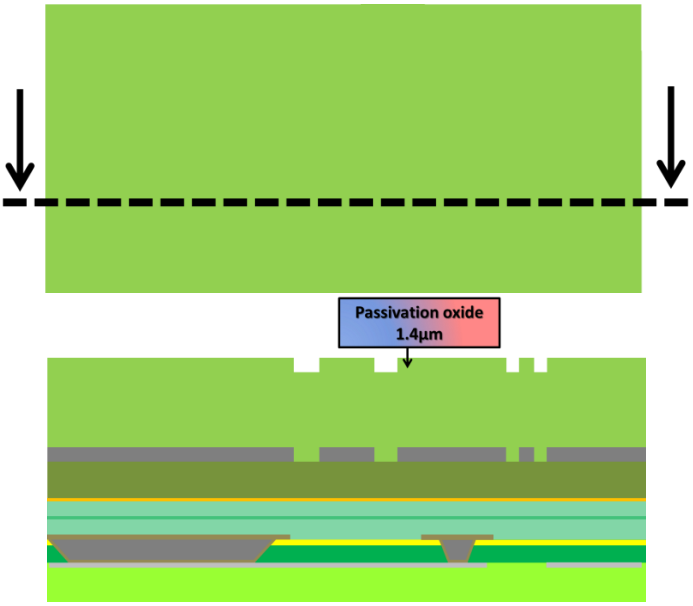


4 Gravure anisotrope du silicium bulk et du BOX (température ambiante).

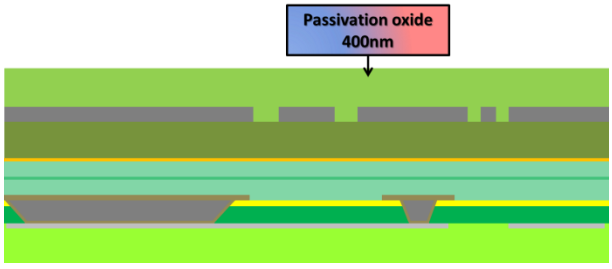
Figure III.2.3: Procédé de fabrication pour les étapes de collage et d'amincissement du silicium.



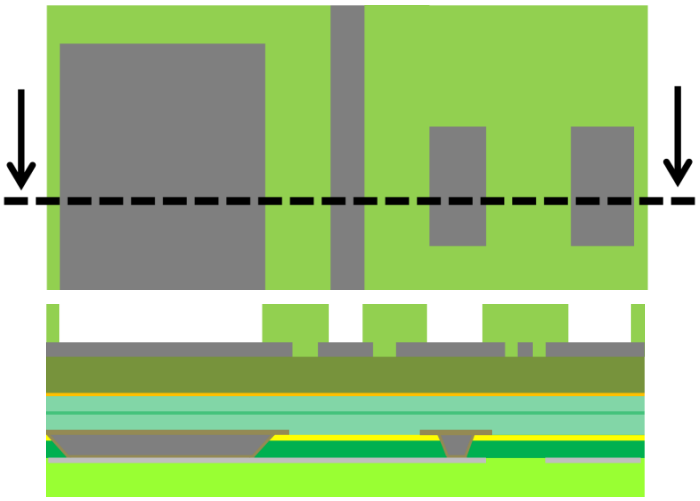
1 Lithographie hybride (DUV et e-beam) et gravure du silicium monocristallin du substrat SOI pour réalisation des résonateurs, du futur routage et des plots métalliques.



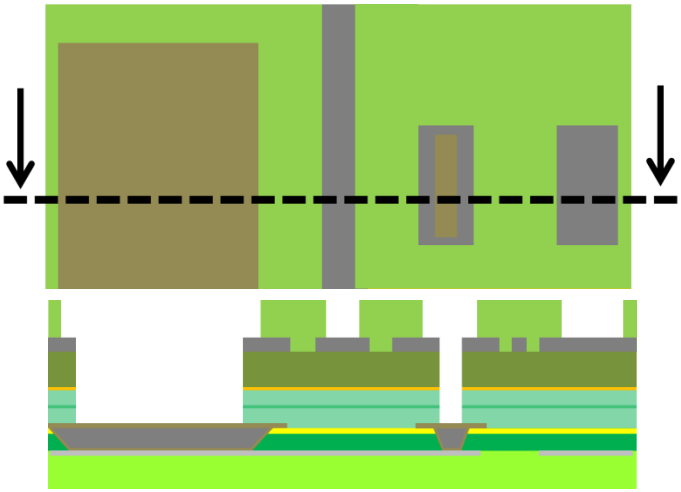
2 Dépôt d'oxyde de passivation (moins de 400°C).



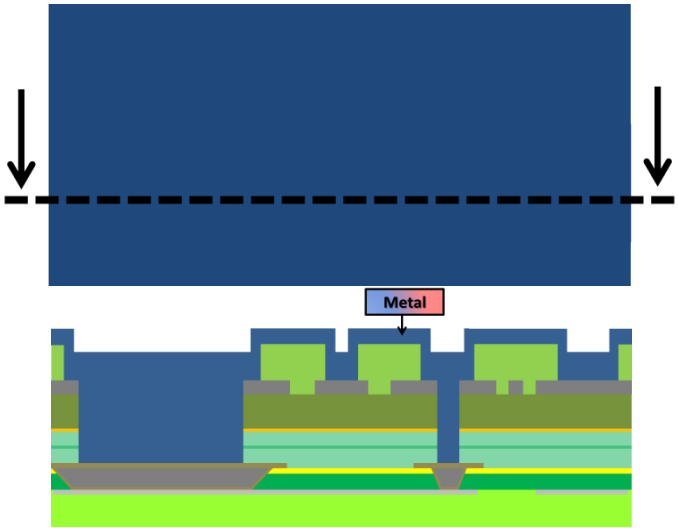
3 Aplanissement de l'oxyde de passivation.



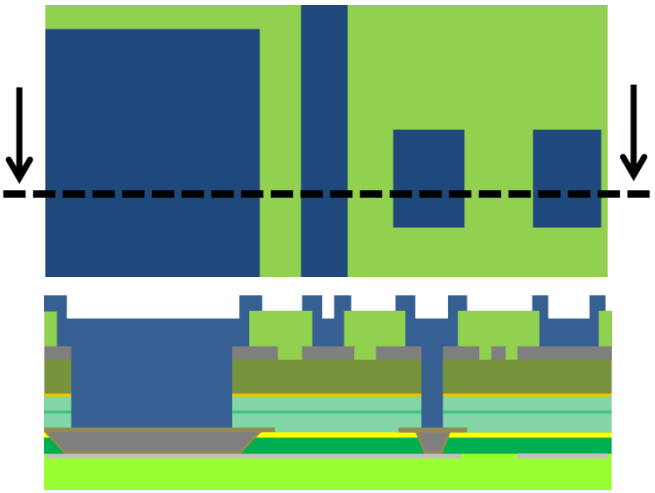
4 Lithographie UV (DUV) et gravure de l'oxyde de passivation pour définition du routage métallique, des vias et des plots.



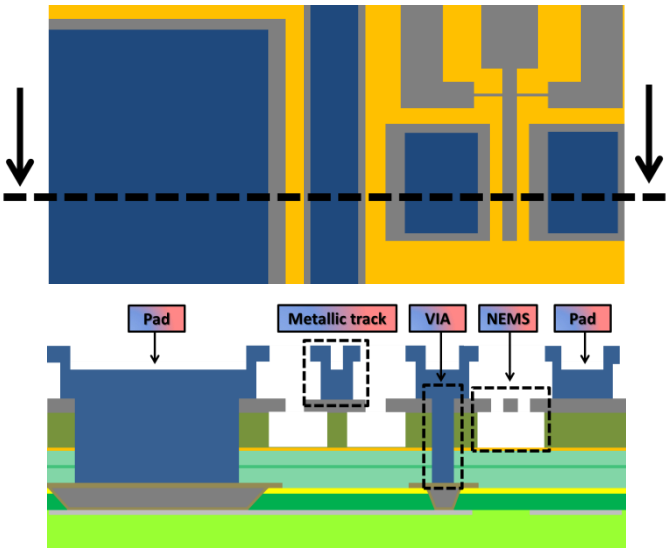
5 Lithographie UV (DUV) et gravure du silicium et de l'empilement de diélectrique avec arrêt sur la barrière Ti-TiN.



6 Dépôt de métal (inférieur à 450°C)



7 Lithographie UV (DUV) et gravure de la couche de métal avec arrêt sur l'oxyde de passivation.



8 Gravure HF (acide fluorhydrique) vapeur et libération des structures NEMS.

Figure III.2.4: Procédé simplifié de réalisation du résonateur et des interconnexions.

III. Etudes de briques technologiques

L'intégration 3D NEMS-CMOS proposée dans le cadre de cette thèse comporte des avantages intéressants. Comme les résonateurs et les interconnexions sont fabriqués après l'assemblage, les contraintes d'alignement restent faibles (en comparaison du collage métal-oxyde).

Trois briques technologiques peuvent être identifiées dans cette intégration et doivent être étudiées et développées (illustrées en Figure III.3.1) :

- Le collage moléculaire entre les substrats SOI et CMOS ;
- L'implémentation des interconnexions entre la partie mécaniques et les niveaux de métal présents dans le substrat CMOS ;
- L'étape de libération des NEMS.

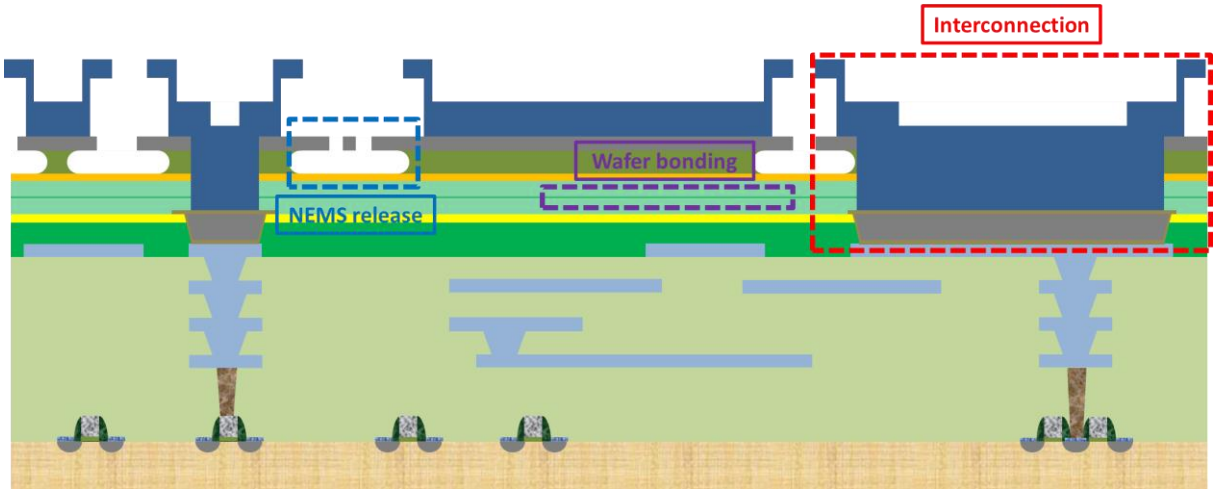


Figure III.3.1: Description des briques technologiques pour le développement de l'intégration 3D NEMS-CMOS "above-IC".

III.1 Libération du NEMS

Cette étape correspond au dernier procédé réalisé dans cette integration. Il consiste à graver l'oxyde présent autour de la structure mécanique sans endommager le résonateur. Cette problématique a été l'objet de plusieurs études [Mul93-Bus94-Hou95-Wil96-Kno00-Kop05-Sav07]. Cependant, la technique la mieux adaptée pour les structures nanométriques reste l'utilisation de la gravure HF vapeur (acide fluorhydrique) [Wit00-Yan06-Rit09-Pol13].

Deux matériaux sont nécessaires pour le développement de l'architecture 3D (voir Figure III.3.2) :

- Une couche sacrificielle à graver pour libérer la structure résonante ;
- Une couche d'arrêt pour stopper la progression de l'HF dans l'empilement et protéger le contenu du substrat CMOS.

L'objectif est maintenant de déterminer les matériaux adéquats pour ces deux couches. Le matériau sacrificiel doit pouvoir être gravé rapidement et sans formation de résidu pour ne pas perturber le mouvement du résonateur. Quant au matériau servant de couche d'arrêt, celui-ci ne doit pas être attaqué par l'HF.

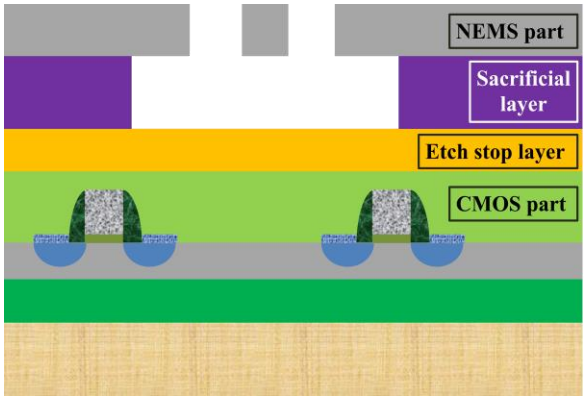


Figure III.3.2: Schéma en coupe simplifié d'une configuration NEMS "above-IC".

III.1.1 – Description de l'expérience

Deux protocoles expérimentaux ont été utilisés. Pour l'étude des matériaux servant de couche sacrificielle (respectivement de couche d'arrêt), des substrats ont été préparés selon le procédé illustré en Figure III.3.3 (respectivement III.3.4). Les différents matériaux étudiés sont répertoriés en Tableau III.1 (respectivement III.2).

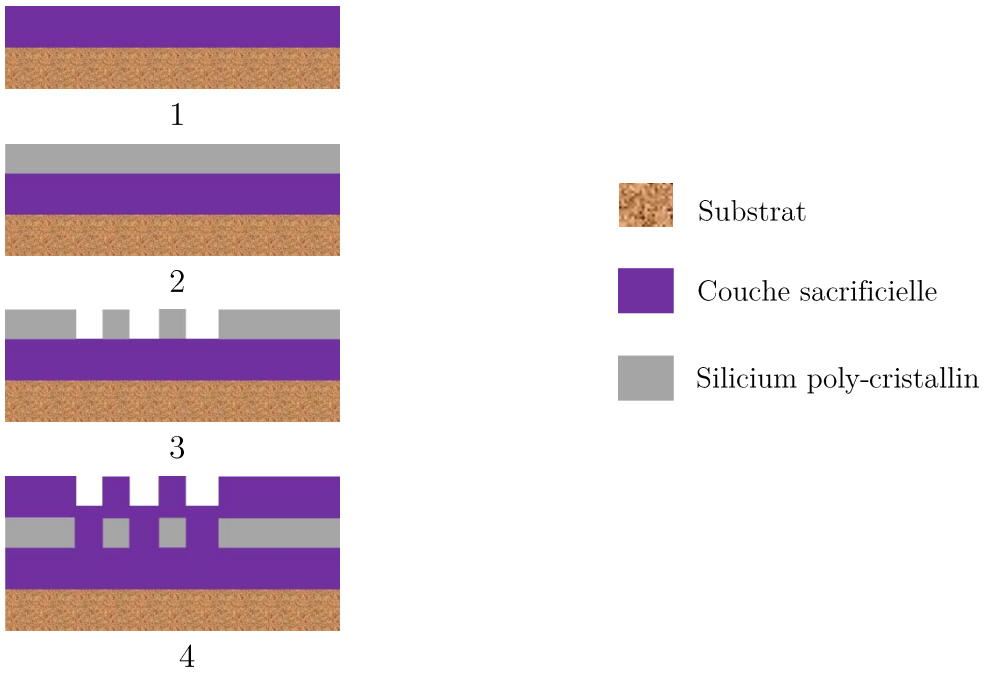
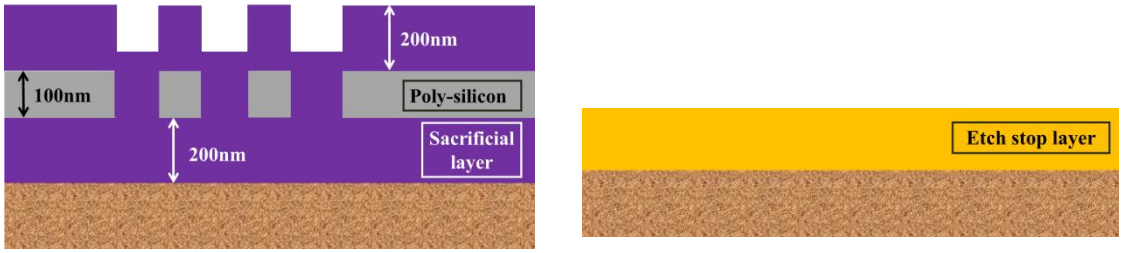


Figure III.3.3: Préparation des substrats pour l'étude des matériaux sacrificiels: (1) dépôt de la couche sacrificielle, (2) dépôt du silicium poly-cristallin, (3) lithographie et gravure d'un réseau de poutres, et (4) dépôt de la couche sacrificielle.

Matériaux	**Méthode de dépôt et température (°C)**
Oxyde de silicium déposé non dopé (USG)	PECVD / 270
Oxyde silane (SiH_4)	PECVD / 400
Oxyde tétra-éthyl-ortho-silicate (TEOS)	PECVD / 400
Oxyde tétra-éthyl-ortho-silicate déposé à faible vitesse (TEOS LR)	PECVD / 400
Oxyde silane de haute densité déposé par voie plasma (HDP SiH_4)	PECVD / 400
Oxyde déposé à haute température (HTO)	LPCVD / 800

Tableau III.1: Caractéristiques des matériaux utilisés pour l'étude de couche sacrificielle.



(a) (b)

Figure III.3.4: Description des substrats servant pour l'étude de couche sacrificielle (a) et de couche d'arrêt (b). Ces deux substrats, après préparation, sont placés sous HF vapeur.

Matériau	Méthode de dépôt et température (°C)
Nitrure déposé à haute température (HTN)	LPCVD / 780
Nitrure de bore (BN)	CVD / 480
Dioxyde d'hafnium (HfO_2)	CVD / 400

Tableau III.2: Caractéristiques des matériaux utilisés pour l'étude de couche d'arrêt.

III.1.2 – Résultats expérimentaux

Deux paramètres sont importants pour la sélection des matériaux en tant que couche sacrificielle et couche d'arrêt : la vitesse de gravure et la présence et les dimensions des résidus pouvant provenir de la formation d'un précipité de fluorure de silicium durant la réaction avec l'HF vapeur [Rit11]. Les vitesses de gravure sont calculées grâce à des mesures ellipsométriques de l'épaisseur avant et après exposition. Les résultats sont montrés en Figure III.3.5. Les dimensions des résidus (voir Figure III.3.6) sont déterminées via des clichés MEB (voir Figures III.3.7 pour les couches d'arrêt et III.3.8 pour les couches sacrificielles).

Les différents résultats montrent que le BN et l'HfO_2 constituent d'excellentes couches d'arrêt à l'HF vapeur puisque ces matériaux présentent une vitesse de gravure nulle et une surface non modifiée après plus d'une heure d'exposition. Quant aux couches sacrificielles, les oxydes TEOS, TEOS LR et HDP SiH_4 montrent des propriétés intéressantes puisqu'aucun résidu n'est formé après 10min de réaction.

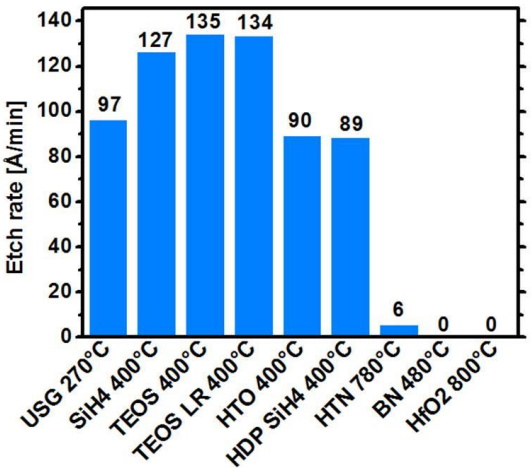


Figure III.3.5: Vitesses de gravure mesurées sur des couches sacrificielles et d'arrêt.

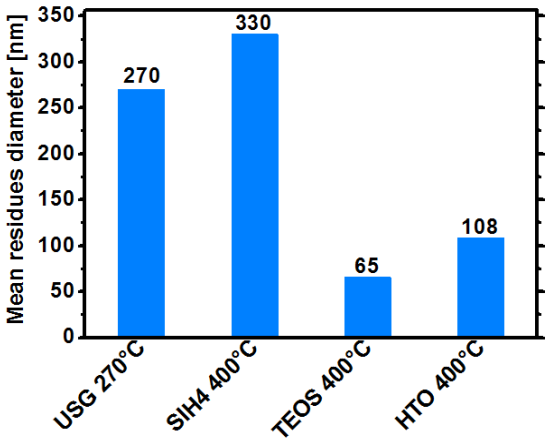
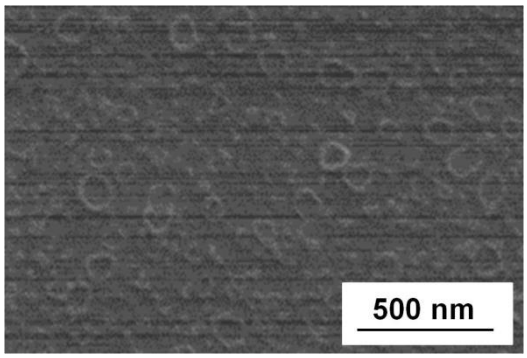
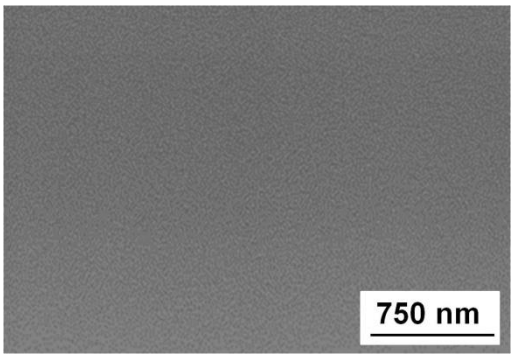


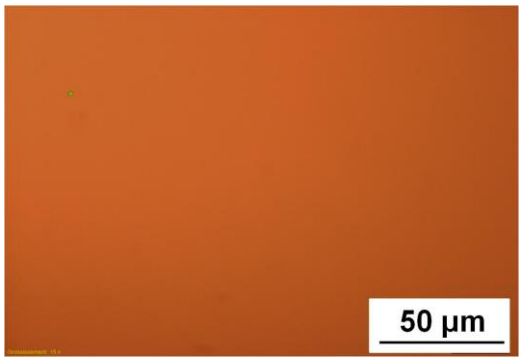
Figure III.3.6: Diamètres moyens des résidus après exposition de l'HF vapeur. Les autres matériaux (TEOS LR, HDP SiH_4, HTN, HfO_2 and BN) n'ont laissé aucun résidu après exposition.



(a)



(b)



(c)

Figure III.3.7: Photographie faite au MEB (a-b) et au microscope optique (c) de couche d'arrêt après gravure. (a), (b) et (c) correspondent respectivement à l'HTN après 10min d'exposition avec une grande présence de cratères en surface, à une couche de BN amorphe après 80min d'exposition avec une surface très propre et une couche cristalline d'HfO_2 après 2h d'exposition avec également une surface très propre.

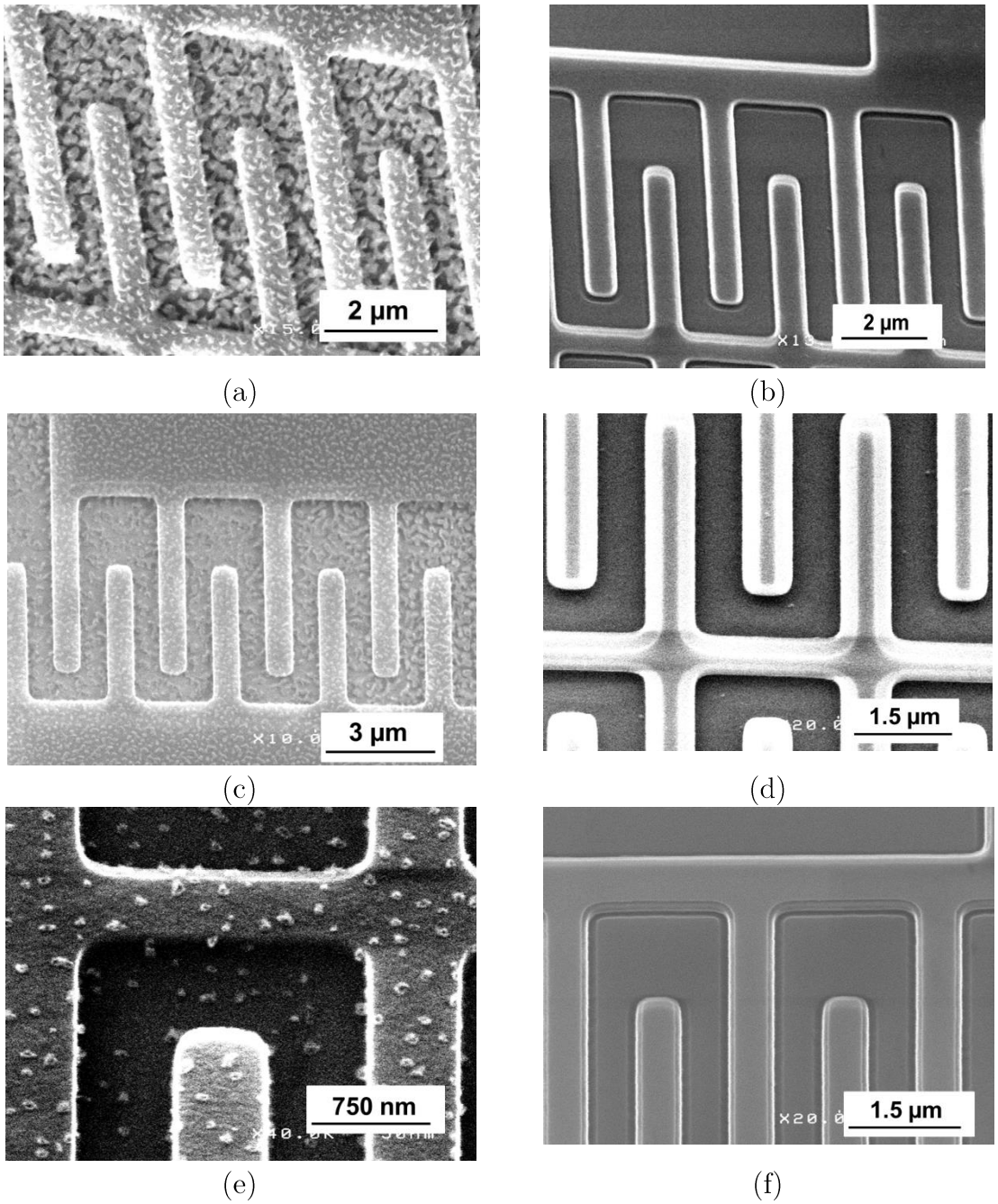


Figure III.3.8: Photographies MEB d'une structure en silicium poly-cristallin comprise entre deux couches sacrificielles (a) de SiH_4; (b) de TEOS LR; (c) de USG; (d) de TEOS; (e) de HTO; (f) de HDP SiH_4.

III.2 Interconnexion NEMS CMOS

Cette section a pour but d'étudier le développement d'un bon contact électrique entre un résonateur NEMS et le circuit CMOS. L'objectif ici est de trouver un métal pouvant remplir des vias de facteur de forme élevé (c'est-à-dire de faible largeur ϕ et de hauteur importante) et résistant à la gravure HF vapeur. D'autre part, la température de dépôt de métal ne doit pas excéder 450°C afin de ne pas dégrader les niveaux de métal déjà présents dans la puce CMOS. De plus, le matériau d'interconnexion doit assurer le contact entre la couche de c-Si et le substrat CMOS avec une faible résistance de contact. Deux dimensions de vias sont étudiées (voir Figure III.3.9).

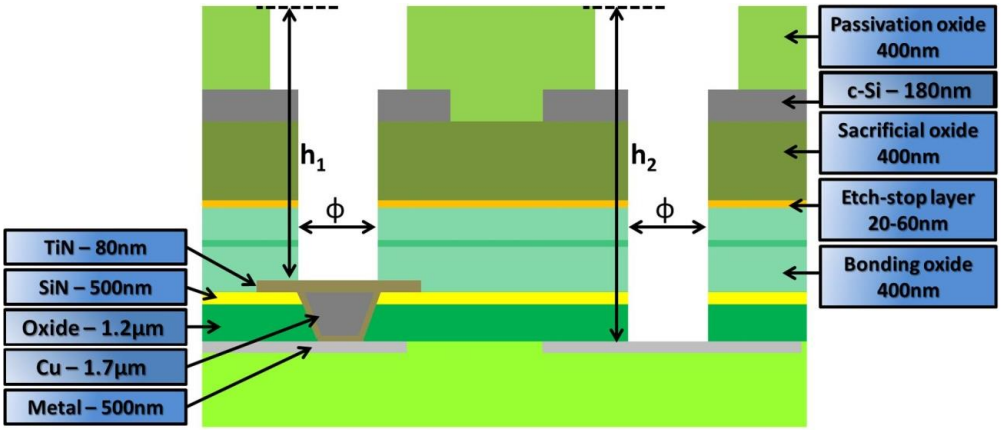


Figure III.3.9: Schéma en coupe des deux types de vias à l'étude. h_1 (=1.4µm) et h_2 (=3.1µm) correspondent respectivement aux profondeurs d'interconnexion entre oxyde de passivation – barrière TiTiN et oxyde de passivation - dernier niveau de métal du substrat CMOS. ϕ représente le diamètre du via.

Avec un procédé de dépôt CVD à une température de 300°C, le WSi constitue un candidat intéressant en raison de sa très bonne conformité (capacité de remplir les vias de facteur de forme élevé), de sa faible résistance de contact avec le silicium [Ohb87]. Cependant, son comportement par rapport à l'HF vapeur n'est pas connu. Dans un premier temps, sa vitesse de gravure sous HF vapeur a été étudiée, puis sa conformité a été comparée à celle d'un autre matériau très utilisé dans l'élaboration de l'interconnexion des NEMS : l'AlSi (déposé en PVD à une température de 175°C).

III.2.1 –Evaluation de la résistance sous HF vapeur

Pour cette étude, deux types d'empilements ont été étudiés (voir Figure III.3.10). La tenue et la perméabilité des matériaux ont été testées sous HF vapeur après différents temps d'exposition. D'après la Figure III.3.11, le WSi possède une excellente résistance à l'HF vapeur puisque ce matériau reste intact et imperméable (oxyde non gravé) même après un temps d'exposition de 1h20

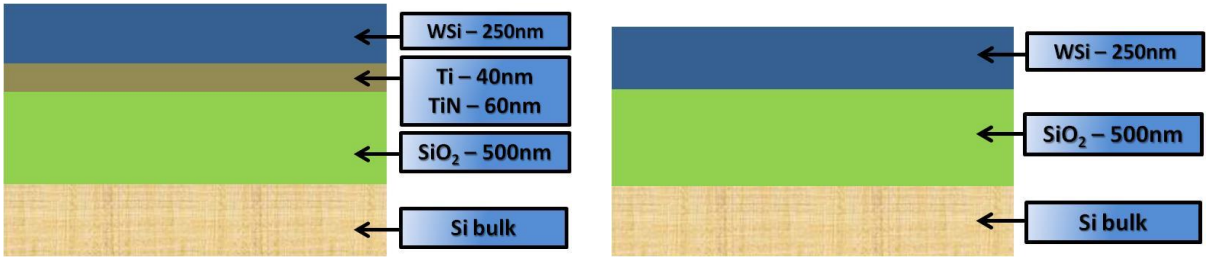
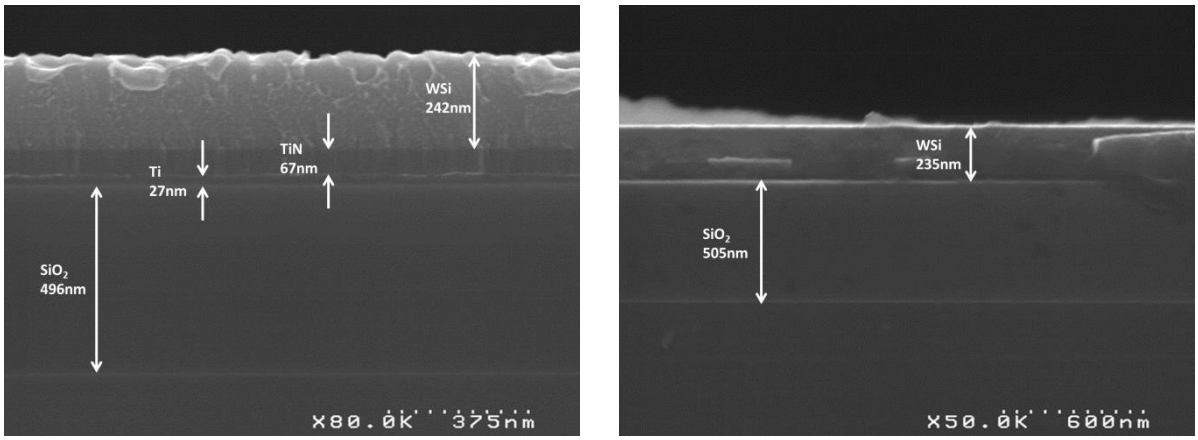
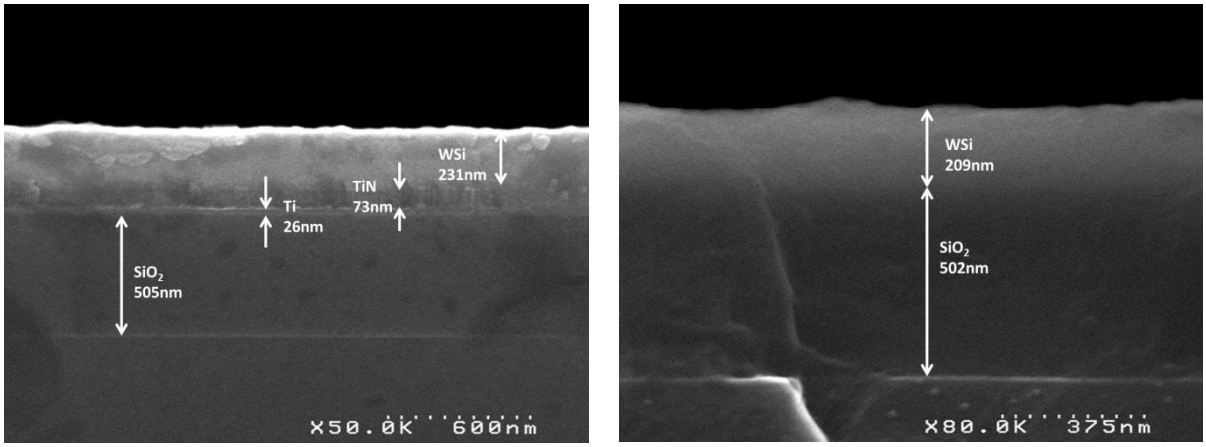


Figure III.3.10: Schéma des empilements étudiés.



Avant exposition



Après exposition de 1h20

Figure III.3.11: Vue en coupe MEB des empilements WSi-TiTiN-SiO_2 et WSi-SiO_2 après exposition sous HF vapeur.

III.2.2 –Evaluation de la conformité

Cette partie traite de l'aspect de conformité de deux métaux: le WSi et l'AlSi. Pour ce faire, des vias de différentes dimensions ont été réalisés, suivi par le dépôt de ces deux matériaux (voir Figure III.3.12). Après remplissage, le caractère conforme des métaux a été évalué à travers des coupes FIB (voir Figure III.3.13 pour l'AlSi et III.3.14 pour le WSi). Les résultats confirment que contrairement à l'AlSi, le WSi permet de remplir des vias de facteur de forme élevé (jusqu'à 1.2 et 1.5µm de diamètre minimum respectivement pour des hauteurs de 1.54 et 3.33µm).

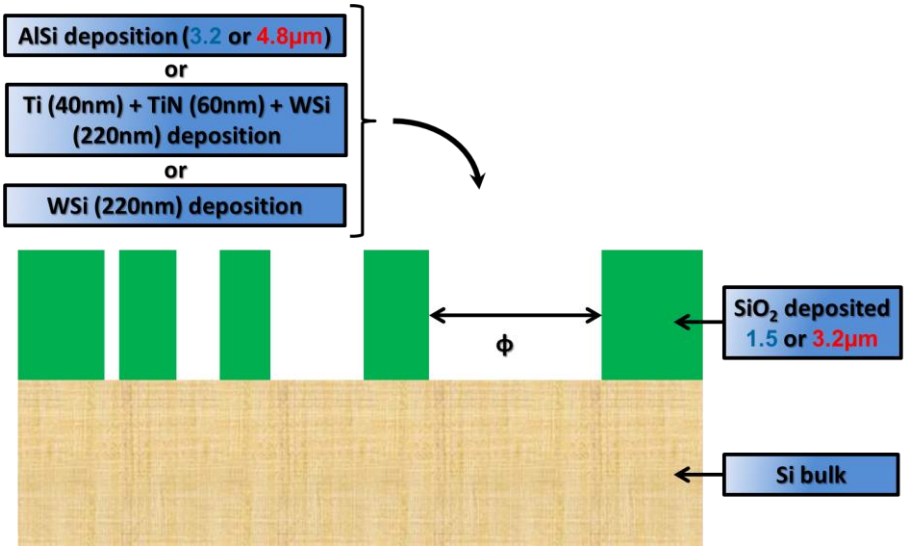
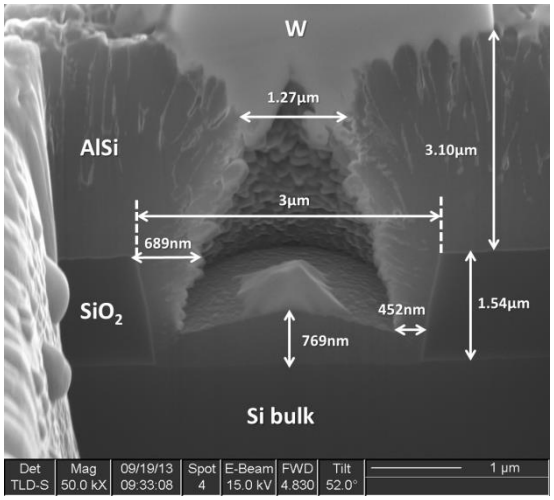
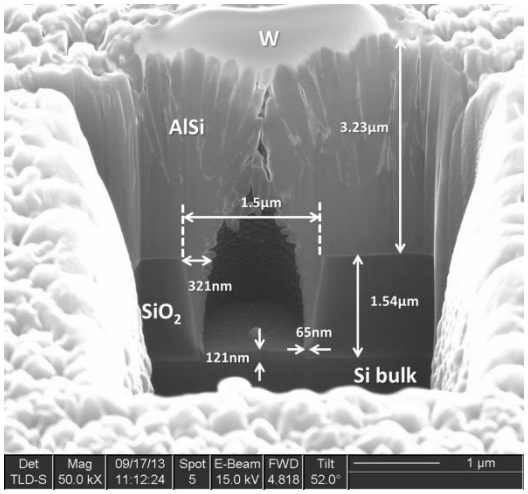


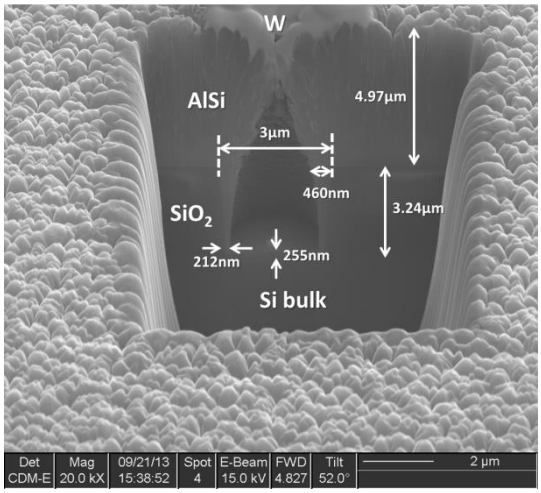
Figure III.3.12: Description schématique du remplissage de via et d'étude de conformité.



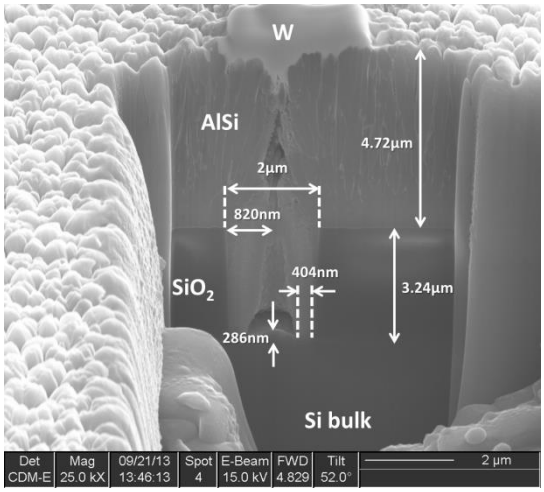
Remplissage d'un via de 3µm de diamètre et de 1,54µm de hauteur.



Remplissage d'un via de 1.5µm de diamètre et de 1,54µm de hauteur.

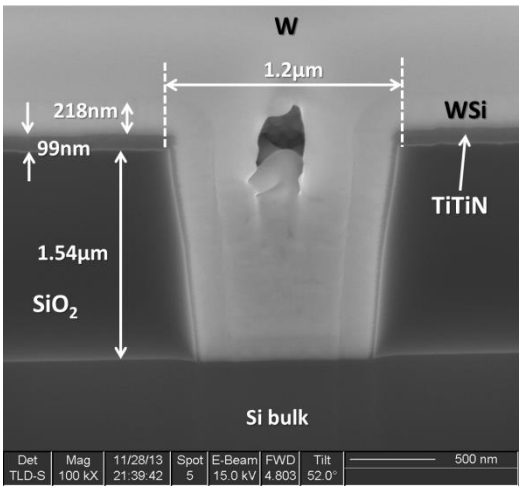


Remplissage d'un via de 3µm de diamètre et de 3,24µm de hauteur.

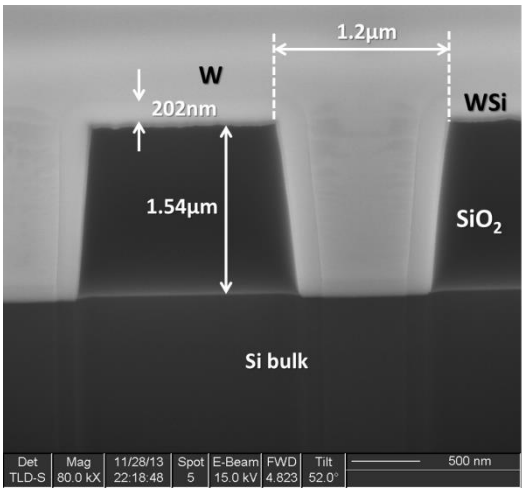


Remplissage d'un via de 2µm de diamètre et de 3,24µm de hauteur.

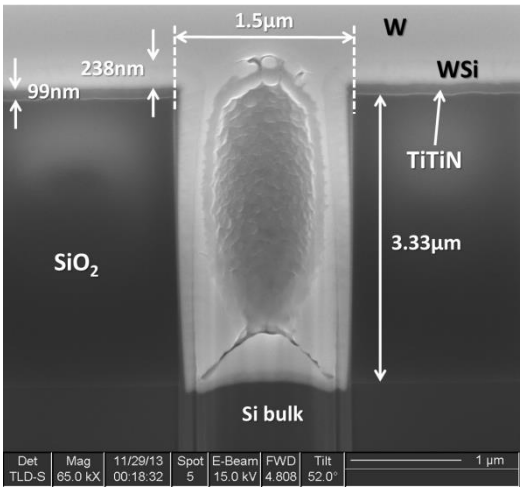
Figure III.3.13: Photographies MEB de remplissage de vias de rapports de forme différents avec de l'AlSi.



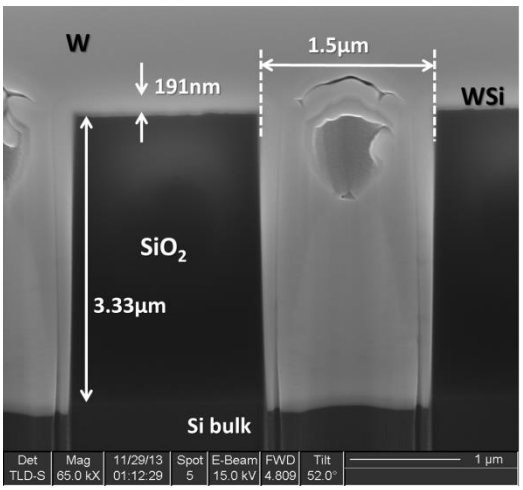
Remplissage d'un via de 1,2µm de diamètre et de 1,54µm de hauteur.



Remplissage d'un via de 1,2µm de diamètre et de 1,54µm de hauteur.



Remplissage d'un via de 1.54µm de diamètre et de 3,33µm de hauteur.



Remplissage d'un via de 1.54µm de diamètre et de 3,33µm de hauteur.

Figure III.3.14: Photographies MEB de remplissage de vias de rapports de forme différents avec du Ti-TiN et du WSi.

III.3 Collage moléculaire

Cette partie expose les résultats relatifs au collage moléculaire entre les plaques SOI et les plaques CMOS suivant le procédé montré en Figure III.2.3. Pour cette étude, des plaques CMOS AMS 0,35µm ne comprenant que le dernier niveau de métal (sur les quatre que propose cette technologie) ont été utilisées. Afin de valider la solidité du collage moléculaire, les plaques collées ont ensuite été l'objet d'un amincissement mécano-chimique du silicium bulk provenant du SOI. Des photographies après amincissement sont montrées en Figure III.3.15. Ces résultats montrent qu'il y a eu délamination du substrat SOI (des motifs du substrat CMOS sont visibles).

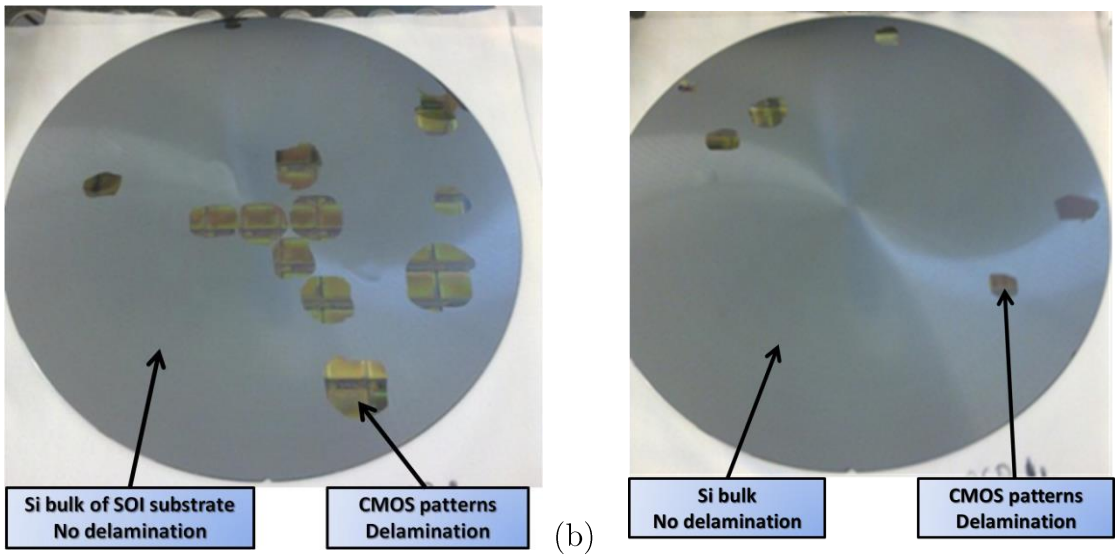
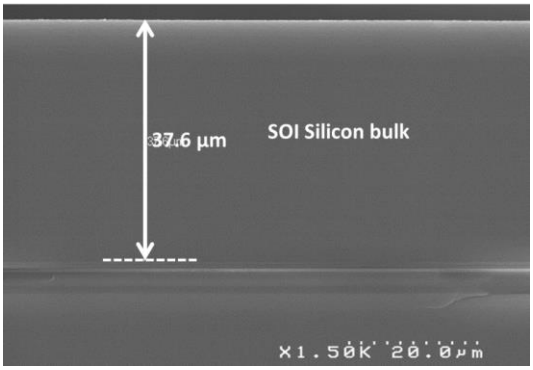
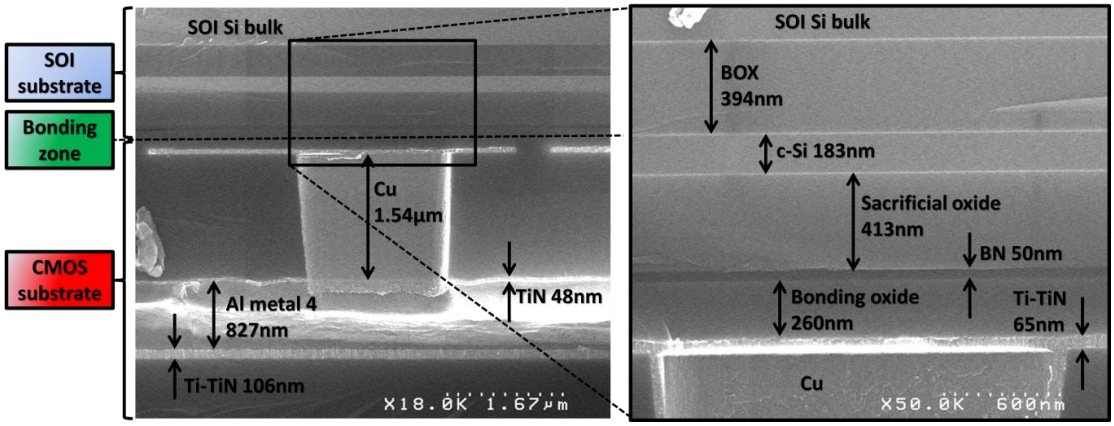


Figure III.3.15: Photographies de substrats collés avec BN (a) et HfO_2 (b) comme couche d'arrêt après polissage mécano-chimique.

L'origine du décollement après polissage doit être analysée. Des vues en coupe réalisées au MEB (Figures III.3.16 et III.3.17) ont permis de montrer que l'interface entre la couche d'arrêt (BN ici) et l'oxyde de collage était en cause. Plusieurs hypothèses permettraient d'expliquer cette délamination : problème de topologie de surface et/ou présence de particules en surface avant collage dû à un nettoyage insuffisant, ou problème d'adhérence de l'oxyde de collage à la couche d'arrêt dont l'énergie d'interface ne serait pas assez élevée pour garantir l'intégrité de l'empilement lors du polissage.



Vue générale du substrat SOI collé sur le substrat CMOS



Zooms à l'interface de collage.

Figure III.3.16: Vue en coupe MEB des substrats CMOS et SOI assemblés par collage moléculaire après polissage.

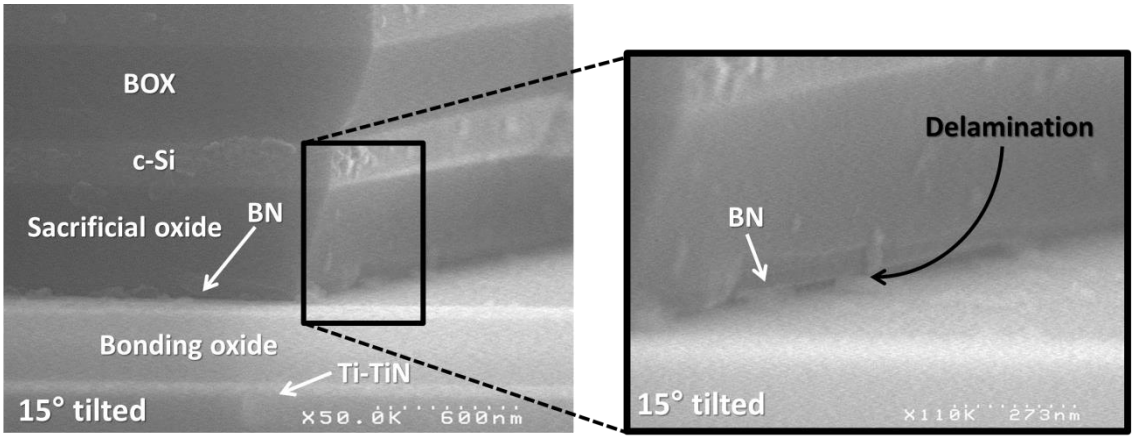


Figure III.3.17: Photographie MEB zoomée sur la zone de délamination.

IV. Discussion et conclusion

Dans ce chapitre a été décrite une stratégie d'intégration monolithique 3D NEMS-CMOS. Cette approche permet d'obtenir un réseau plus dense de résonateurs en comparaison avec l'exemple traité dans le chapitre II. Trois briques technologiques ont été identifiées et étudiées :

- Le collage moléculaire a démontré une fragilité de l'empilement provenant de l'interface entre la couche d'arrêt et l'oxyde de collage ;
- L'étude de la libération de la structure NEMS a démontré l'intérêt des oxydes TEOS, TEOS LR et HDP SiH_4 en tant que couche sacrificielle et les diélectriques BN et HfO_2 en tant que couche d'arrêt ;
- L'interconnexion entre la partie NEMS et la partie CMOS peut être réalisé grâce au WSi qui semble être un excellent matériau pour cette brique technologique grâce à sa résistance à l'HF vapeur et à son caractère conforme.

Cette approche est intéressante puisque peu d'étapes sont nécessaires à la réalisation du capteur. Il est néanmoins possible de faciliter davantage le procédé de fabrication en utilisant des substrats CMOS sans ouverture sur les niveaux sur le métal et dont la surface est à priori plane. Seules des opérations de lithographie et gravure seraient nécessaires lors de la réalisation du via et ce, sans recourir à des opérations de polissage du cuivre.

Afin de pouvoir optimiser la densité du réseau de NEMS, nous devons également aborder la partie design qui sera l'objet du chapitre suivant.

Chapitre IV

Considérations de design pour la co-intégration NEMS-CMOS

Les chapitres précédents ont permis de découvrir un exemple d'auto-oscillateur basé sur une co-intégration 2D et le développement d'une intégration monolithique 3D. L'aspect design constitue également un point crucial pour la fabrication des capteurs. Cette partie est l'objet de ce dernier chapitre.

I. Contexte

Les considérations de dessin ne concernent qu'un type de dispositif NEMS-CMOS avec les caractéristiques suivantes :

- Les nano-résonateurs sont fait en c-Si;
- Les structures utilisées sont des "crossbeam" (voir chapitre 1);
- Les systèmes mécaniques sont libérés à l'HF vapeur;
- Les plots métalliques ne sont pas inclus.

Deux architectures en particulier respectent ces critères : la co-intégration 2D et la co-intégration 3D avec les NEMS fabriqués en « above-IC ».

II. Co-intégration 2D NEMS-CMOS

II.1 Introduction

Six dimensions sont à considérer pour l'implémentation de cette intégration (voir Figure IV.2.1) :

- La distance entre les niveaux de métal d'interconnexion et les résonateurs NEMS notée $d_{metal\text{-}NEMS}$;
- La distance entre deux lignes de métal du même niveau (noté i^{eme}): $d_{metal\ i\ -\ metal\ i}$;
- La longueur et la largeur de l'espace occupé par une ligne de métal (du i^{eme} niveau) respectivement notées $L_{metal\ i}$ and $w_{metal\ i}$;
- La longueur et la largeur de l'ouverture faite dans l'empilement diélectrique du back-end pour accéder aux résonateurs et les libérer: L_{NEMS} and w_{NEMS}.

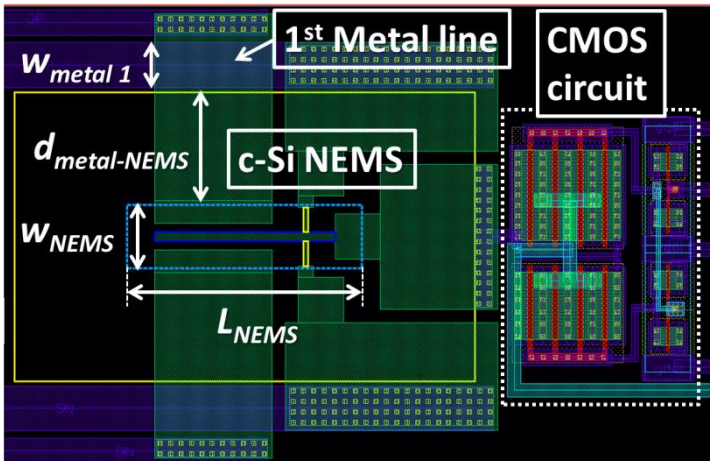


Figure IV.2.1 Vue layout d'un exemple d'intégration NEMS-CMOS en 2D.

II.2 Construction du réseau de NEMS

$d_{metal\ i\ -metal\ i}$ et $w_{metal\ i}$ ont chacune une valeur minimum fixée qui dépend de la technologie CMOS utilisée. Les autres dimensions n'ont pas de limite puisque la réalisation et la libération des NEMS a lieu en dehors du procédé CMOS. La valeur de ces paramètres dépend des contraintes de fabrication. Une certaine distance doit être respectée entre l'ouverture faite dans l'empilement diélectrique et les interconnexions métalliques. Cette distance tient compte de la vitesse de gravure de ces diélectriques et du temps d'exposition à l'HF vapeur, celui-ci ne devant pas atteindre le métal d'interconnexion. Un exemple de réseau standard de NEMS est illustré en Figure IV.2.2. Un moyen d'améliorer la densité du réseau est de faire partager les ouvertures du back-end et les électrodes de plusieurs résonateurs, comme indiqué en Figure IV.2.3.

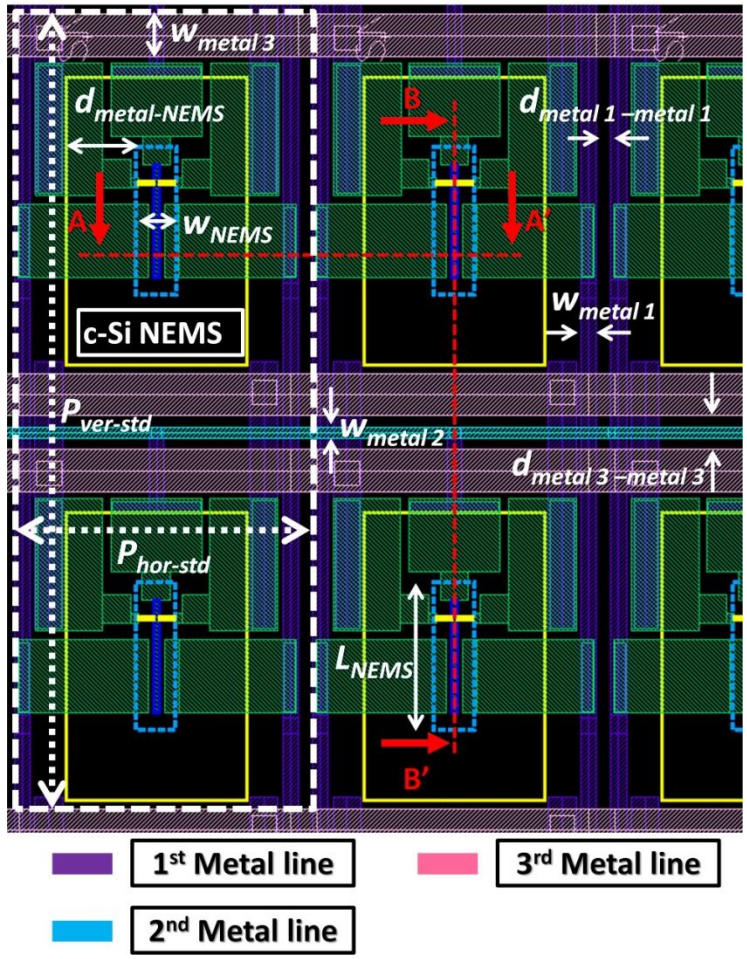


Figure IV.2.2: Vue layout d'un réseau standard de NEMS avant libération.

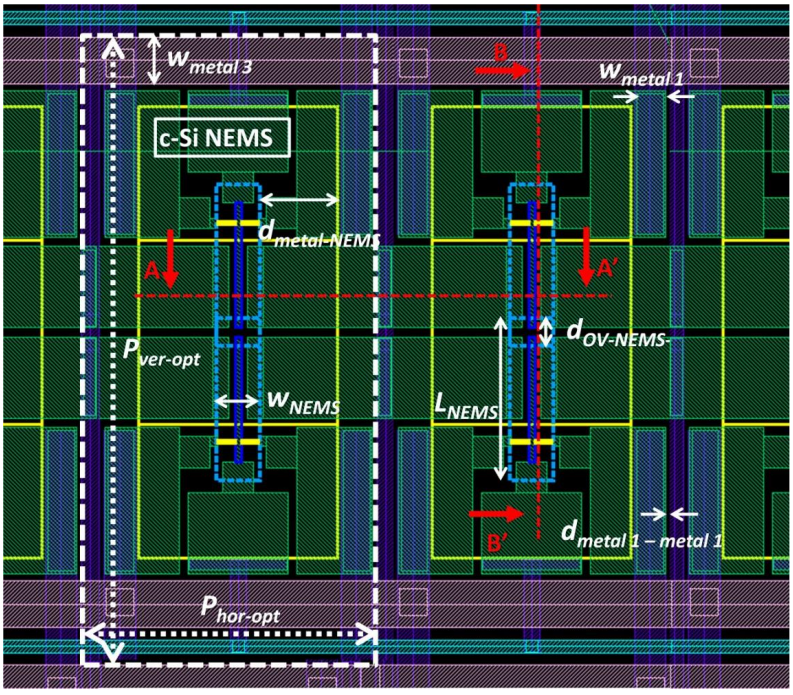


Figure IV.2.3: Vue layout d'un réseau optimisé de NEMS avant libération.

II.3 Evaluation de la compacité du capteur

Cette section s'intéresse à la détermination de la surface occupée par le réseau de résonateur, plus particulièrement par un réseau de deux NEMS (voir Figure IV.2.2 et IV.2.3). Ici, les pas horizontaux (P_{hor}) et verticaux (P_{vert}) du réseau sont évalués pour une configuration standard (Figure IV.2.2) et optimisée (Figure IV.2.3). Leurs expressions sont données ci-dessous:

$$P_{hor-st} = 4w_{metal1} + 3d_{metal1-metal1} + 2d_{metal1-NEMS} + w_{NEMS} \ [\mathrm{m}] \quad \text{(IV.1)}$$

$$P_{ver-st} = 3w_{metal3} + d_{metal3-metal3} + 4d_{metal3-NEMS} + 2L_{NEMS} \ [\mathrm{m}] \quad \text{(IV.2)}$$

$$P_{hor-op} = 3w_{metal1} + 2d_{metal1-metal1} + 2d_{metal-NEMS} + w_{NEMS} \ [\mathrm{m}] \quad \text{(IV.3)}$$

$$P_{ver-op} = 2w_{metal3} + d_{metal3-metal3} + 2d_{metal3-NEMS} + 2L_{NEMS} - d_{OV-NEMS-NEMS} \ [\mathrm{m}] \quad \text{(IV.4)}$$

Les valeurs des différentes dimensions sont indiquées en Tableau IV.1. L'évaluation des pas permet de déterminer de l'aire occupée par le réseau de deux NEMS (notée $A_{2\text{-}NEMS\text{-}array}$) ainsi que le nombre de résonateurs présents sur une puce de 1mm^2 (noté N_{NEMS}).

$$A_{2-NEMS-array} = P_{hor} \cdot P_{ver} \ [\mathrm{m}^2] \quad \text{(IV.5)}$$

$$N_{2-NEMS-array} = \frac{A_{die}}{A_{2-NEMS-array}} \quad \text{(IV.6)}$$

$$N_{NEMS} = 2 \cdot N_{2-NEMS-array} \quad \text{(IV.7)}$$

Nom	L_{NEMS}	w_{NEMS}	$d_{metal\ i\ -\ metal\ i}$	$w_{metal\ i}$	$d_{metal\ i\ -\ NEMS}$	$d_{OV\text{-}NEMS\text{-}NEMS}$
Valeur [µm]	15	1	0.5	0.5	1.5	1

Tableau IV.1: Valeurs des dimensions prises pour l'analyse de la compacité du résonateur.

Le Tableau IV.2 résume les résultats obtenus pour les deux types de configuration. En partageant des électrodes et les ouvertures à travers le back-end, une réduction de 24% de la surface occupée est obtenue.

Intégration		**2D NEMS-CMOS**
Configuration standard	Pas entre deux réseaux de deux NEMS	$P_{hor\text{-}st} = 7.5\mu m$ $P_{vert\text{-}st} = 38\mu m$
	Aire et nombre maximal de réseaux de deux NEMS sur une puce de $1mm^2$	$285\mu m^2$ / 3508
	Nombre maximal de NEMS sur une puce de $1mm^2$	7016
Configuration optimisée	Pas entre deux réseaux de deux NEMS	$P_{hor\text{-}op} = 6.5\mu m$ $P_{vert\text{-}op} = 33.5\mu m$
	Aire et nombre maximal de réseaux de deux NEMS sur une puce de $1mm^2$	$217.75\mu m^2$ / 4592
	Nombre maximal de NEMS sur une puce de $1mm^2$	9184

Tableau IV.2: Aire occupée par des réseaux de NEMS dans le cas d'une co-intégration 2D.

III. Co-intégration 3D NEMS-CMOS en configuration “above-IC”

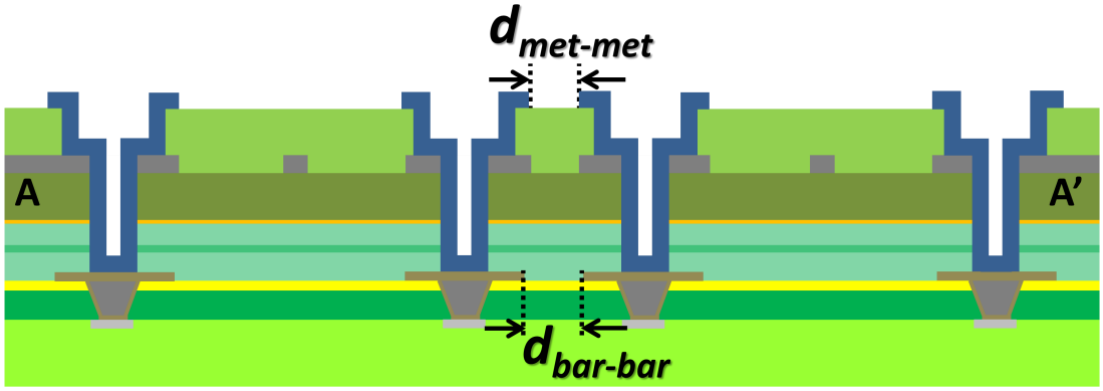
III.1 Introduction

La partie mécanique étant implémentée au-dessus du circuit et des interconnexions électroniques, une plus grande compacité des réseaux de résonateur est attendue. Cette section se propose d'analyser les solutions pour augmenter le nombre de résonateurs en surface et ainsi maximiser la surface de capture du détecteur.

III.2 Construction du réseau de NEMS

Sans tenir compte des restrictions sur les interconnexions du back-end CMOS, deux dimensions doivent être prises en compte et peuvent affecter la densité du réseau : le pas minimum entre deux barrières TiN (noté $d_{bar\text{-}bar}$) et entre deux lignes de métal supérieur (noté $d_{met\text{-}met}$). La Figure IV.3.1 correspond à une illustration d'un réseau standard de résonateurs NEMS. Tous les éléments des nano-résonateurs (électrodes d'actionnement, de détection et de sortie) sont connectés au CMOS à travers les vias réalisés avant la libération des structures mécaniques. Comme dans la première partie, il est possible de réduire la place occupée par le résonateur en mettant des électrodes en commun comme illustré dans la Figure IV.3.2 dans laquelle les électrodes de détection et d'actionnement sont partagées.

(a)



(b)

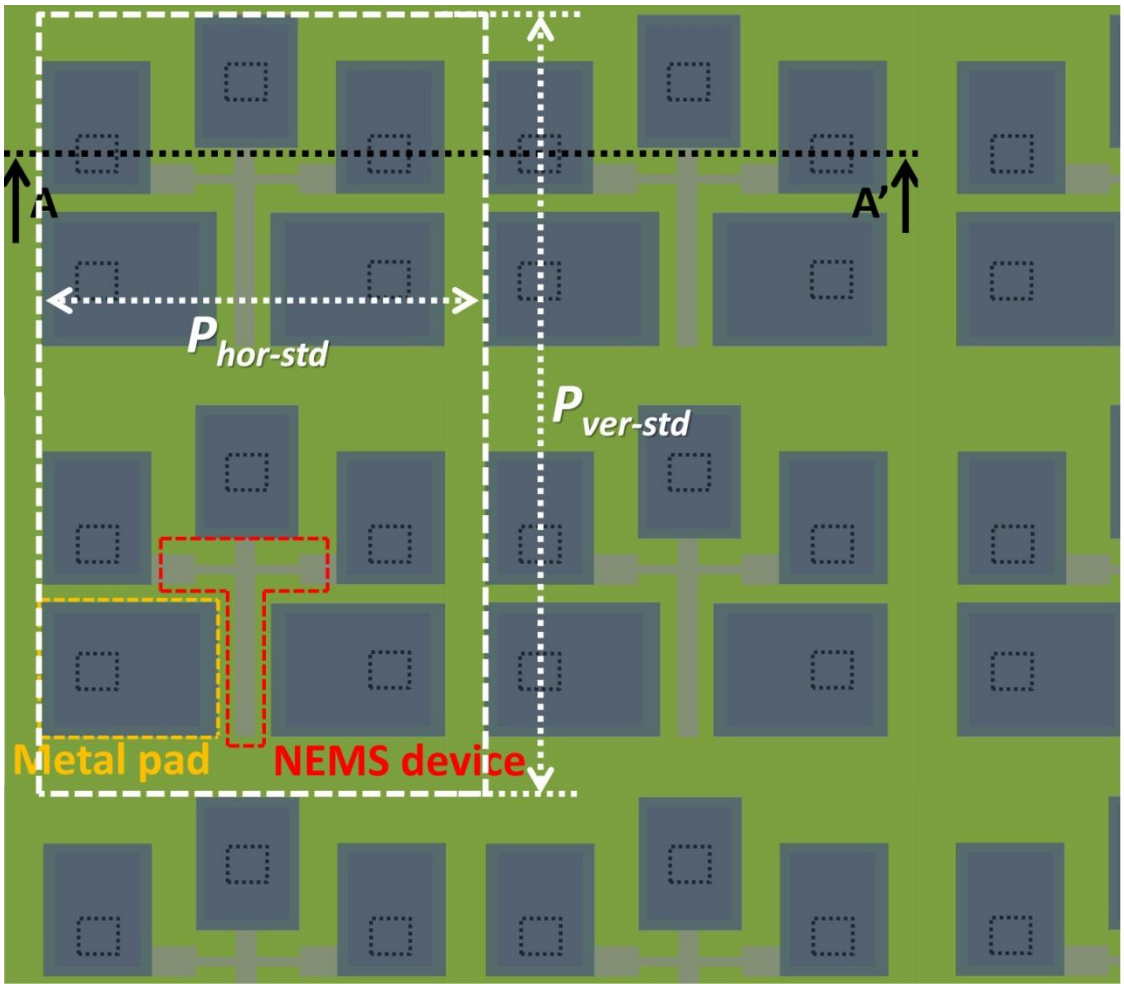
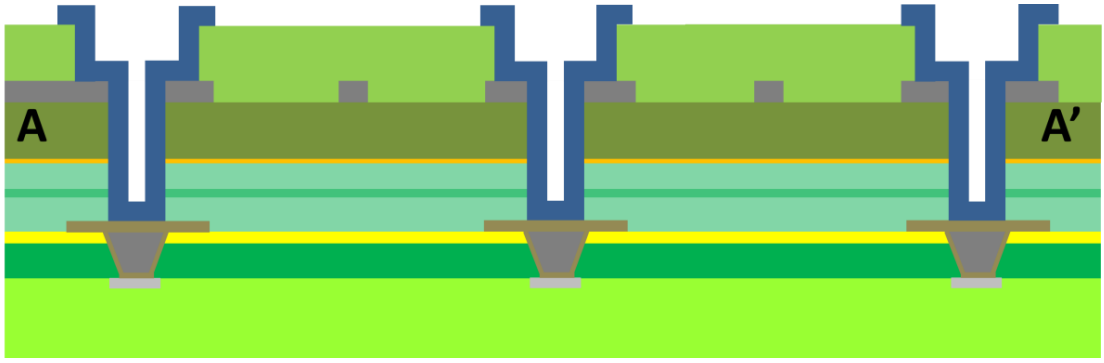


Figure IV.3.1: Vue schématique en coupe (a) et de dessus (b) d'un réseau standard de résonateur.

(a)



(b)

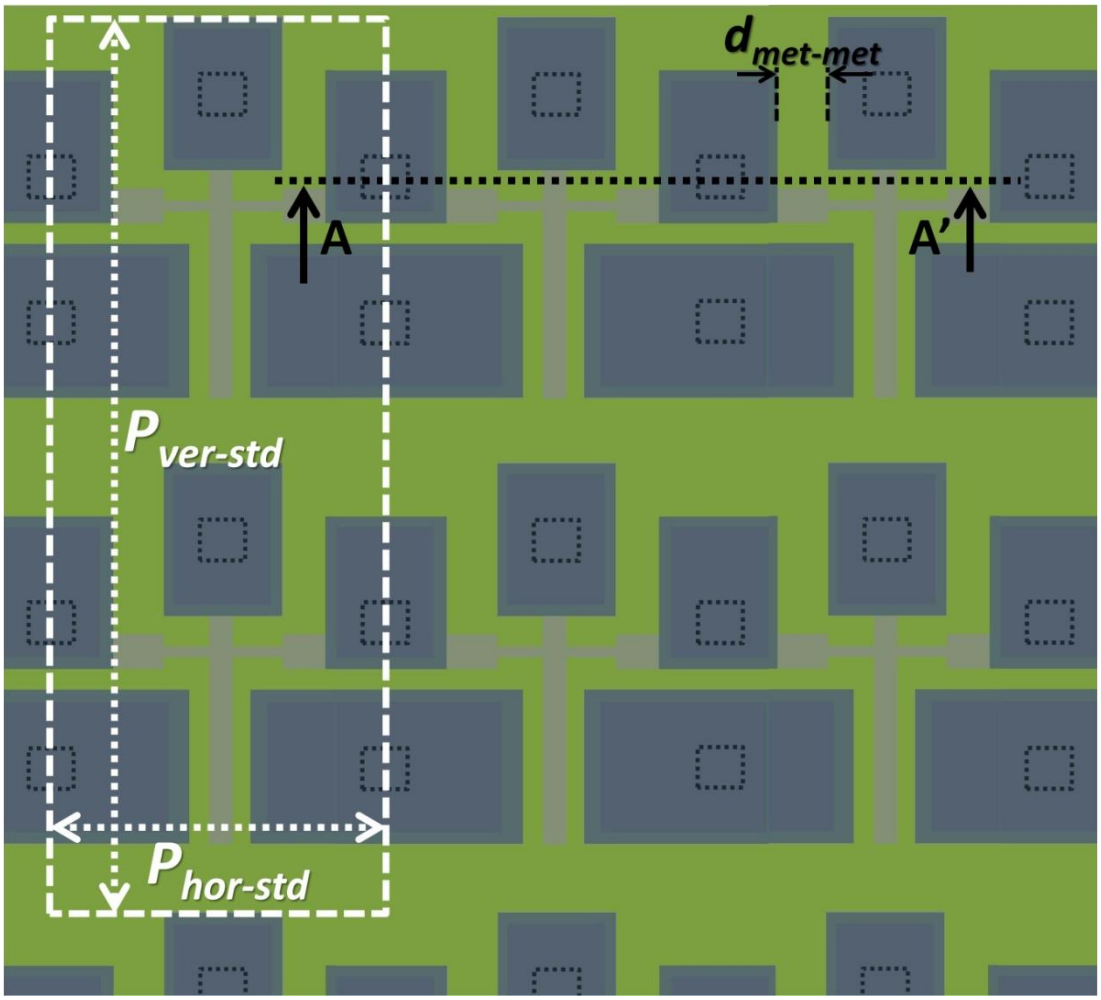


Figure IV.3.2: Vue schématique en coupe (a) et de dessus (b) d’un réseau optimisé de résonateur.

III.3 Evaluation de la compacité du capteur

L'analyse présentée dans la seconde partie est également conduite pour l'intégration 3D « above-IC ». Les expressions des différents pas sont données ci-dessous. Les pads de détection, d'actionnement et de sortie sont de forme carrée et de surface notée S_{met}.

$$P_{hor-st} = 2\sqrt{S_{met}} + d_{metal-metal} + w_{NEMS} \quad \text{(IV.8)}$$

$$P_{ver-st} = 2\sqrt{S_{met}} + 2L_{beam} + 2d_{metal-metal} \quad \text{(IV.9)}$$

$$P_{hor-op} = \sqrt{S_{met}} + w_{NEMS} \quad \text{(IV.10)}$$

$$P_{ver-op} = 2\sqrt{S_{met}} + 2L_{beam} + 2d_{metal-metal} \quad \text{(IV.11)}$$

Les valeurs des différentes dimensions sont indiquées en Tableau IV.3. L'évaluation des pas permet la détermination de l'aire occupée par le réseau de deux NEMS (notée $A_{2\text{-}NEMS\text{-}array}$) ainsi que le nombre de résonateurs présents sur une puce de 1mm² (noté N_{NEMS}) grâce aux équations ci-dessous.

Nom	L_{beam}	w_{NEMS}	$d_{metal-metal}$	$\sqrt{S_{met}}$
Valeur [µm]	10	1	0.5	2

Tableau IV.3: Valeurs des dimensions prises pour l'analyse de la compacité du résonateur.

Le Tableau IV.4 résume les résultats obtenus pour les deux types de configuration. En mettant en commun les électrodes d'actionnement et de détection, une réduction de 45% de la surface occupée par le réseau est obtenue.

Intégration		3D NEMS above-IC
Configuration standard	Pas entre deux réseaux de deux NEMS	$P_{hor\text{-}st}$ = 5.5µm $P_{vert\text{-}st}$ = 25µm
	Aire et nombre maximal de réseaux de deux NEMS sur une puce de 1mm²	137.5µm² / 7272
	Nombre maximal de NEMS sur une puce de 1mm²	14544
Configuration optimisée	Pas entre deux réseaux de deux NEMS	$P_{hor\text{-}op}$ = 3µm $P_{vert\text{-}op}$ = 25µm
	Aire et nombre maximal de réseaux de deux NEMS sur une puce de 1mm²	75µm² / 13333
	Nombre maximal de NEMS sur une puce de 1mm²	26666

Tableau IV.4: Aire occupée par des réseaux de NEMS dans le cas d’une configuration 3D NEMS « above-IC ».

IV. Discussion et conclusion

Ce chapitre a proposé une analyse concernant le design d’un réseau de résonateurs co-intégré avec un circuit CMOS. Celle-ci a démontré l’intérêt de l’intégration monolithique 3D pour la conception d’un capteur de haute densité de NEMS. La mise en commun de plusieurs électrodes entre différents résonateurs constitue une possibilité intéressante pour augmenter la compacité du détecteur et ainsi augmenter la surface de capture.

Conclusion et perspectives

Après divers développements technologiques, les MEMS sont devenus de plus en plus incontournables de par leur présence dans de nombreux objets de notre vie quotidienne. La miniaturisation de ces objets vers les dimensions nanométriques ont permis l'émergence des NEMS et de nouvelles applications exigeant à la fois une sensibilité et une précision élevée, tels la spectrométrie de masse et les capteurs de gaz. L'utilisation de résonateurs NEMS pour la détection de masse requiert cependant la mise en place de réseau d'un très grand nombre de résonateurs ainsi que l'utilisation de circuit électronique CMOS nécessaire pour constituer un capteur travaillant en temps réel. Ce circuit a pour but de traiter le signal en sortie de résonateur et d'implémenter une boucle oscillante. La mise en oscillation des structures résonantes et la détection des variations de fréquence d'oscillation permet la constitution d'un capteur de masse. Le silicium monocristallin, de par ses excellentes propriétés électromécaniques, s'avère être un matériau de premier choix pour la réalisation des résonateurs.

Le chapitre I a permis de dresser différentes solutions pour intégrer la partie NEMS avec la partie CMOS. La solution monolithique apparaît comme étant la meilleure approche par rapport à l'approche dite hybride. Malgré les contraintes imposées lors de la fabrication, la co-intégration sur la même puce des parties NEMS et CMOS génère beaucoup moins de capacités ainsi que beaucoup moins d'étapes de fabrication. Deux types d'intégration permettent d'utiliser le silicium monocristallin en tant que couche structurante pour les nano-résonateurs : une co-intégration 2D et une co-intégration 3D dite « above-IC » dans laquelle les éléments mécaniques sont fabriqués au-dessus du circuit électronique et des interconnexions.

Dans le second chapitre, la démonstration d'un oscillateur à base d'une cellule 2D NEMS-CMOS a été réalisée. L'utilisation d'une boucle–oscillante a permis de fabriquer un dispositif très compact avec un circuit composé seulement de sept transistors. Ce dispositif NEMS–CMOS constitue une structure intéressante pour la constitution de détecteur de masse. Il est possible d'optimiser la surface occupée en passant d'une co-intégration 2D à une co-intégration 3D.

Un procédé de fabrication de co-intégration 3D NEMS–CMOS dans laquelle la partie mécanique est réalisée au-dessus des interconnexions CMOS a été présenté dans le troisième chapitre. Cette technologie fait apparaître trois modules technologiques :

- ❖ Le collage moléculaire entre une plaque CMOS et une plaque SOI servant à la préparation des résonateurs. L'interface entre couche d'arrêt et oxyde de collage semble être le point faible de l'empilement et nécessite davantage de travail pour l'améliorer.
- ❖ L'interconnexion entre les parties NEMS et CMOS a également été étudiée. Le WSi semble être un matériau adéquat pour garantir la connexion électrique entre la couche de silicium supérieure et les niveaux métalliques du circuit. Sa résistance de contact avec le silicium est de bonne qualité. D'autre part, ce matériau est inerte à l'HF vapeur et peut remplir des vias de fort facteur de forme.
- ❖ L'étude de la libération à l'HF vapeur a permis de dégager des matériaux pour les couches sacrificielles comme les oxydes TEOS, TEOS LR et SiH_4 HDP, ainsi que pour les couches d'arrêt, comme le BN et l'HfO_2.

Cette intégration peut être améliorée grâce au caractère conforme du WSi. En effet, il serait possible de faire la gravure de l'empilement diélectrique jusqu'au niveau du dernier niveau de métal du substrat CMOS pour la réalisation des vias. Ce même substrat ne nécessiterait alors aucune ouverture au niveau de ce niveau, simplifiant le procédé de fabrication (plus de dépôt cuivre et plus d'étape d'aplanissement nécessaire). Le collage moléculaire étant une opération difficile et coûteuse (substrats SOI chers), une alternative consisterait à procéder à des dépôts de couches pour la construction du nano-résonateur. Les températures de dépôt et de recuit thermique (si nécessaire) ne devraient en revanche pas excéder le budget thermique maximum des interconnexions CMOS.

Afin d'augmenter la surface de capture des molécules, le chapitre IV a permis de voir que le partage des électrodes entre différents résonateurs permet d'augmenter le nombre de NEMS sur une puce pour une configuration 3D « above-IC ». Il est cependant nécessaire d'analyser la fonctionnalité d'un tel arrangement. L'endommagement d'un résonateur (au niveau de la détection par exemple) pourrait en effet affecter d'autres dispositifs, voir le réseau tout entier, rendant cette configuration moins effective que la version standard (sans partage d'électrode). Une analyse supplémentaire permettrait d'arriver à un compromis entre fonctionnalité et densité du réseau.

Cette thèse a permis de voir plusieurs aspects de la co-intégration entre NEMS et CMOS, particulièrement l'assemblage technologique, l'architecture du circuit et l'aspect design. L'analyse de la technologie 3D monolithique « above-IC », l'étude de la conception de réseau dense de résonateurs NEMS et la démonstration expérimentale d'un auto-oscillateur NEMS-CMOS rendent ces dispositifs hybrides prometteurs pour les applications de détection de masse.

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Technologie de fabrication et analyse de fonctionnement d'un système multi-physique de détection de masse à base de NEMS co-intégrés CMOS

Résumé :
Ces dernières décennies ont vu l'émergence des microsystèmes électromécaniques (MEMS) grâce notamment aux techniques de fabrication employées dans l'élaboration des transistors. L'utilisation de différentes propriétés physiques (électroniques, mécaniques, optiques par exemple) a permis la construction d'un large panel de capteurs miniaturisés. Résultant de la miniaturisation sub-micrométrique des MEMS, les nanosystèmes électromécaniques (NEMS) constituent un tout nouveau type d'objet permettant d'adresser des applications nécessitant un très haut niveau de sensibilité et de résolution, comme la détection de gaz, la spectrométrie de masse ou la reconnaissance de molécules faisant traditionnellement appel à des machines très volumineuses. L'utilisation de ces NEMS requiert cependant un circuit électronique CMOS afin de lire et d'exploiter le signal en sortie de résonateur et servant également à la mise en place d'une boucle oscillante (boucle à verrouillage de phase ou boucle auto-oscillante par exemple), architecture idéale pour la détection de masse en temps réel. L'intégration du circuit CMOS avec les résonateurs NEMS constitue un aspect critique quant à la fabrication de capteurs de haute performance. La solution optimale consiste à intégrer de manière monolithique ces deux parties sur la même puce, permettant ainsi de réduire la dimension du capteur et d'améliorer la transmission du signal électrique entre les résonateurs et le circuit CMOS. Cette thèse propose dans un premier temps d'analyser l'intérêt de cette co-intégration du point de vue électrique. Dans un second temps, cette thèse portera sur le développement d'une approche originale visant à co-intégrer de manière monolithique les nano-résonateurs au-dessus du circuit CMOS et des interconnexions. La dernière partie portera sur le design d'un détecteur de masse composé d'un réseau compact de NEMS co-intégré CMOS.

Mots clés: NEMS, CMOS, co-intégration, détection de masse, fabrication, caractérisation

Technology development and analysis of a multiphysic system based on NEMS co-integrated with CMOS for mass detection application

Abstract :
During these last decades, Very Large Scale Integration (VLSI) techniques, well developed for transistors, have been used for the Micro ElectroMechanical Systems (MEMS) devices. Thanks to the combination of different physical properties (such as electronic, mechanical, optical etc.) the fabrication of various kinds of miniaturized sensors has been made possible. The sub-µm downscaling of MEMS has allowed the emergence of a new kind of devices called NEMS (for Nano ElectroMechanical Systems) and the possible use of the electromechanical systems in specific applications in which a high level of sensitivity and resolution is necessary, such as gas sensing, mass spectrometry and molecules recognition, to replace traditional bulky machines. Nevertheless, the use of these NEMS requires a CMOS electronic to enhance NEMS resonators readout and to implement closed-loop oscillators (e.g. phase-locked loop or self-oscillating loop) that provide real-time mass measurements. The integration of the electronic circuit with the resonators is a critical aspect for the fabrication of high performance sensors. The best way consists in monolithically processing these two parts on the same die allowing a size reduction of the sensor and an optimal signal transmission between the NEMS resonators and the CMOS circuit. In a first time, this thesis proposes to analyze the interest of this co-integration from an electrical point of view. In a second time, this thesis deals with the development of a 3D co-integration in which the nano-resonators are fabricated above the CMOS circuit and the interconnections. The final part is focused on the layout design considerations for the implementation of a compact mass sensor based on a NEMS array co-integrated with a CMOS.

Key words: NEMS, CMOS, co-integration, mass sensor, fabrication, characterization